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WOCSDICE 94

18th EUROPEAN WORKSHOP ON COMPOUND SEMICONDUCTOR DEVICES AND INTEGRATED CIRCUITS

WOCSDICE '94

KINSALE, IRELAND

29 May - 1 June 1994

Organised by: Optronics Ireland
National Microelectronics Research Centre
University College Cork

WOCSDICE 94

Proceedings of

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Invited Speakers:

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Program

Session 1:	Materials and Characterisation *Chair:* *H. Hartnagel*	Mon 30 May am
Session 2:	Modelling / Simulation *Chair:* *E. Kohn*	Mon 30 May am
Session 3:	Transistors 1 *Chair:* *V. Morgan*	Mon 30 May pm
Session 4:	OEICs *Chair:* *H. Thim*	Mon 30 May pm
Session 5:	Transistors 2 *Chair:* *L. Eastman*	Tue 31 May am
Session 6:	Two Terminal Devices *Chair:* *W.M. Kelly*	Tue 31 May am
Session 7:	Integrated Devices *Chair:* *F. Fantini*	Wed 1 June am
Session 8:	Optical Devices *Chair:* *D. Pavlidis*	Wed 1 June am

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Session 1: Materials and Characterisation:

Chair: H. Hartnagel (Technische Hochschule Darmstadt)

1. **Hideki Hasagawa** (Invited)
   Hokkaido University — Japan
   Low-damage fabrication technologies of nanostructures for devices in quantum regime

2. **D.Pavlidis**, C.-H. Hong and K.Wang
   University of Michigan — USA
   Growth and material characteristics of cubic GaN on GaAs substrates

3. A.Castaldini, A.Cavallini, C.Del Papa, C.Canali, **F.Nava**, C.Frigeri, A.Cetronio, C.Lanzieri
   Universities of Bologna and Modena, MASPEC, Alenia — Italy
   Deep levels in semi-insulating gallium arsenide determined by PICTs

4. **B.K.Jones**, Gongjiu Jin, M.A.Iqbal
   Lancaster University — UK
   The surface state trap in GaAs FETs

5. **C.R.Whitehouse** (Invited)
   Sheffield University — UK
   X-Ray imaging of strained layers

6. **J.D.Lambkin**, A.Morrison, L.Considine, G..M.O'Connor, C.McDonagh
   NMRC, University of Galway — Ireland
   Energy-band structure of type I and type II InGaP/InAlP short period superlattices

7. **D.V. Morgan**, S.Morgan
   University of Wales — UK
   Low resistance ohmic contacts to GaAs using ion assisted deposition

8. **J.Hayes**, J.O'Brien, J.Braddell, W.M. Kelly
   NMRC — Ireland
   Fabrication of submicron gratings for 1.55μm DFB lasers using DRYDEL process

Low-Damage Fabrication Technologies of Nanostructures for Devices in Quantum Regime

Hideki Hasegawa

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It is expected that all the microelectronic devices go into quantum mechanical regime at the turn of the century as a result of continued scaling-down of device dimensions. Intensive efforts are now being made at present to establish new technologies to realize quantum structures including quantum wells, wires and dots that may become basic building blocks of next generation nanoelectronics. In quantum regime, motions of electrons are far more delicate and sensitive to defects as compared with the average classical motions of electrons in the present-day devices. Particularly, defects at surfaces and interfaces play far more important roles in nanostructures. Thus, the key issue is how to realize defect-free structures with well-controlled surfaces and interfaces.

The purpose of this paper to present and discuss the present status of the development of low-damage fabrication technologies of nanostructures. A brief overview of various approaches of nanostructure fabrication is given at first. Then, specific approaches that are currently pursued at the Research Center for Interface Quantum Electronics are presented and discussed.

The topics include (1)GaAs/InGaAs quantum structure formation by selective MBE and selective MOVPE growth on masked and patterned substrates, (2)interface control in quantum structures and (3)in-situ electrochemical process for direct Schottky contact formation to quantum well and its applications.

Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)
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Growth and Material Characteristics of Cubic GaN on GaAs Substrates

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Abstract

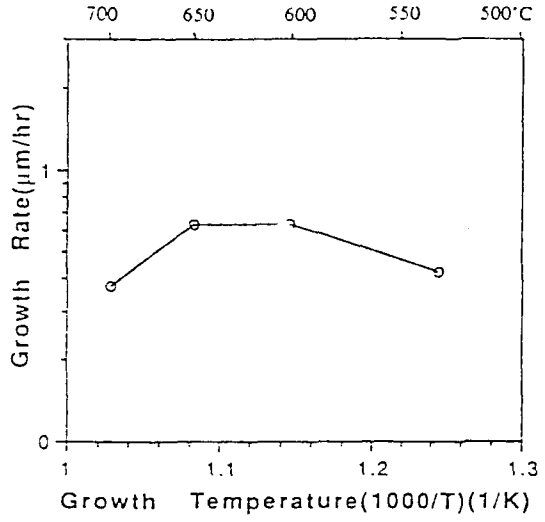
Nitride-based compound semiconductors open new possibilities for optoelectronic and electronic applications. The base compounds GaN, AlN and InN and combination of them are direct semiconductors covering a wide range of bandgaps varying from 1.9 eV to 6.2 eV. It is consequently interesting to envisage use of such semiconductors for blue to ultra-violet wavelength optical components and high temperature devices. A major handicap in growing nitrides has been the lack of suitable substrates. Sapphire and Si have traditionally been used but present a high lattice mismatch of the order of 13 and 17%, respectively. Moreover these substrates are not directly compatible with GaN in terms of crystal structure and material grown on them has been reported to be hexagonal(wurtzite). This paper reports the growth of GaN on a more compatible crystalline structure, namely GaAs. Lattice mismatch on such substrates is high(20.9%) but it is shown that cubic(zincblende) instead of hexagonal material can be obtained. In addition to obtaining cubic material which is more suitable for electronic applications, one can also envisage use of the GaAs substrate for integrating other optoelectronic components.

The GaN films were grown by in-house low-pressure(60 torr) metallorganic-chemical vapor phase deposition (MOCVD). The GaAs substrate surface was first prepared by treatment in H_2 and AsH_3 at 650°C to remove the surface oxide. After nitridation with the surface being exposed to NH_3 only, TMGa and NH_3 were supplied simultaneously and films were grown in the temperature range of 530°C to 700°C. The maximum growth rate obtained in the mass-transport limited regime(600~650°C) was 0.6μm/hr with a V/III ratio of 3000.

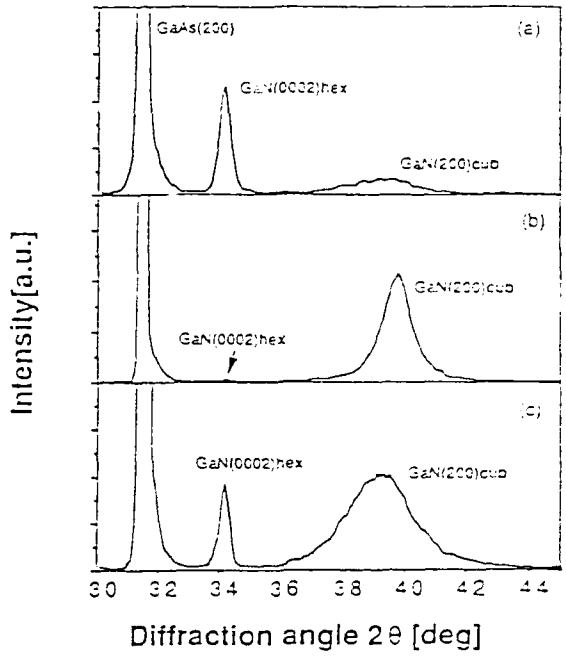
Cubic GaN material growth was obtained by growing at a temperature of 600°C. This was confirmed by X-ray diffraction(XRD) which revealed a cubic peak $(200)_{cub}$ at $2\theta=39.8°$. The use of temperature above or below the range of 600°C to 650°C resulted in simultaneous presence of a peak at $2\theta= 34.3°$ which is related to (0002) hexagonal or (111) cubic GaN. The FWHM of the $(200)_{cub}$ peak was of the order of 1°. The lattice constant extracted from the XRD spectrum was 4.528Å. Unlike previous reports which have been limited to cathodoluminesence characteristics, the films revealed photoluminescence spectra in the temperature range of 6.5 to 77K. The dominant peak was at 3.366eV and is related to bandedge emission. Its FWHM was 5.3meV. The GaN film quality was also confirmed by Raman spectroscopy characterization. The results showed a strong longitudinal phonon(LO) peak at 728cm^{-1}, as well as, a peak at 558 cm^{-1} assigned to transverse optical phonon(TO) mode.

Overall cubic GaN material has been obtained on (100) GaAs substrates and promising characteristics has been demonstrated by XRD,PL and Raman spectrum characteristics.

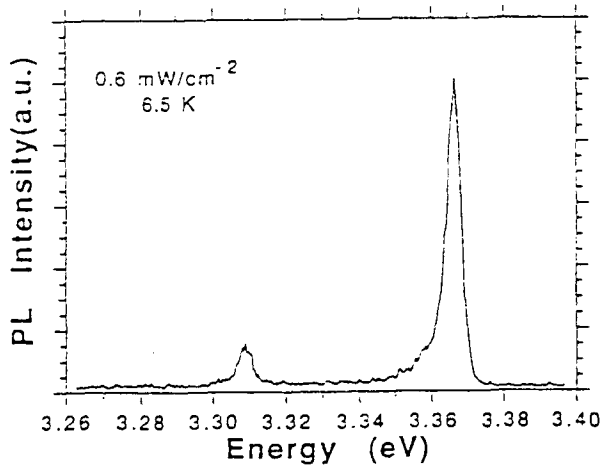
Work supported by ONR Contract No. N00014-92-J1552



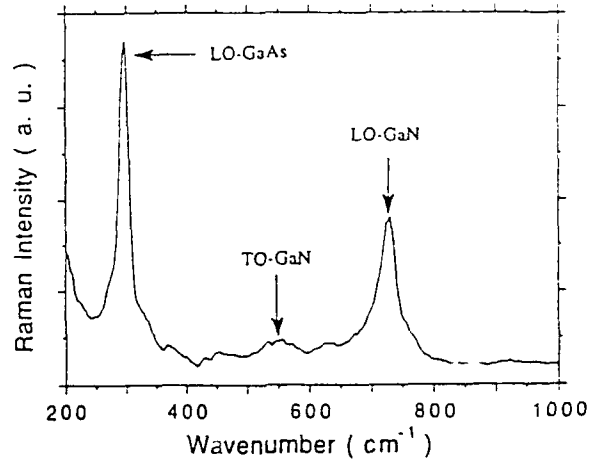
Growth rate of GaN on (100) GaAs as a function of temperature. Maximum growth rate is 0.6μm/hr



X-ray diffraction patterns of GaN grown on (100) GaAs at (a) 530°C, (b) 600°C and 670°C. Cubic (200) GaN formation is dominant at 600°C.



Photoluminescence of cubic GaN on (100) GaAs. The spectrum shows bandedge(3.366eV) and D-A recombination features.



Raman spectrum of cubic GaN on (100) GaAs. Strong longitudinal optical(LO) phonon observed at 728cm^{-1}

Deep Levels in Semi-Insulating GaAs determined by PICTS

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The electrical properties of semi-insulating (SI) GaAs are very sensitive to residual impurities and defects because of the width of the band gap: deep lying centres are necessary to capture and compensate the excess carriers. While there is an extensive literature on deep levels in GaAs and on their effects on device characteristics when used in the fabrication of fast integrated logic or microwave devices, only few references exist on the trapping effects on the particle detectors characteristics, namely on their charge collection efficiency.

In the present work we applied optical transient spectroscopy (OTS), also known as photo-induced current transient spectroscopy (PICTS) to undoped LEC starting material from various manufacturers. One of these manufacturers provided us with wafers taken from different positions of the same ingot.

Due to the interest caused by the evident correlation between presence of trapping centres and charge collection efficiency of particle detectors elsewhere reported, this paper deals with position in the band gap and concentration of trapping centres, which have been investigated by modified PICTS. The analysis of both the dark current and the photocurrent has been performed. In order to allow an accurate determination of the trap position in the forbidden gap, the energy levels have been found by both the best fits of the PICTS profiles and the relevant Arrhenius plots.

Experimental evidence for the presence of five traps has arisen, whose densities have been carefully determined by the procedure of Tapiero et al [1] taking into account absorption, quantum efficiency and carrier mobility/lifetime product and their dependence on temperature.

On the basis of the trap depths and the trap types as determined by the PICTS technique and through a comparison with the main deep centres observed in semiconducting LEC GaAs by the DLTS (Deep Level Transient Spectroscopy) technique, the possible identities of some of the main traps are here presented and the most suspicious ones for charge collection efficiency behaviour are discussed.

1. Tapiero M, Benjelloun, Zielinger J.P., El Hamd S. and Noguet C. J. Appl. Phys. 64 (1988) 4006

The surface state trap in GaAs

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Many transient, time dependent, frequency dependent and low frequency noise effects are observed in GaAsFETs. One of the most important of these is the surface, hole-like, traps since it has a time constant of about 1msec at room temperature.

Detailed studies have been made of all the traps in several GaAsFETs. The techniques used have included conductance DLTS, mutual conductance dispersion, low frequency noise, DLTS characterisation spectroscopy all in the channel ohmic regime. Other complementary studies such as backgating and substrate current oscillations have also been performed. All the data were taken between 77K and 360K.

A brief review of the characteristics (Activation energy and trap cross-section) will be given together with their known location. Two electron-like traps with a weak effect are found in the n-channel. An important hole-like trap is found at the surface of the ungated GaAs channel and many hole-like traps are located in the substrate.

Most of the discussion will concentrate on the properties of the surface trap (E =0.6eV and σ =6x10exp-15 cm2

Its location at the surface has been verified by its observation in different experiments and at different biases. Two special experiments have been performed to demonstrate this. The DLTS experiment on a dual gate device has shown the expected effects when operated with either one gate or both connected together. The direct correlation between the noise in the gate leakage current and in the drain current has shown to be correlated only for this trap so that the leakage current flows through a surface channel modulated by the trap occupancy which also modulates the depletion region and hence the channel width.

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ABSTRACT

A rapidly increasing number of III-V device structures now incorporate pseudomorphically strained component layers, either to overcome the lack of an appropriate lattice-matched substrate for the specific device wavelength required, or to exploit strain-induced changes in band-structure. In addition, over the past years, there has been a major interest in the growth of highly-mismatched multilayer combinations (eg GaAs on Si, InSb on GaAs, InP on GaAs etc.) in order to exploit the multi-device functionality thus offered.

With this ever-increasing usage of mismatched material combinations, it is becoming very important to gain a detailed understanding of the strain relaxation processes involved in order to optimise the design, reliability and operating flexibility of next-generation devices. Whilst many laboratories currently use techniques such as X-ray diffractometry, electron microscopy, photoluminescence, Raman, RBS, etc, to sense strain relaxation, many of these techniques are actually relatively insensitive to the onset of relaxation and also fail to provide the necessary physics information required to understand the relaxation process.

The present paper will describe the important strain-relaxation data which can be provided by the X-ray topography (XRT) technique. XRT is able to sense the formation of the very first strain-relieving dislocation across an entire full-sized device wafer, and hence provide the first genuine values for critical thickness. In addition, XRT can provide the necessary Burgers vector information regarding the specific strain-relief processes involved. The technique is non-destructive, and, unlike electron microscopy, does not need any specialised sample thinning process which could influence the observed dislocation geometries. Following growth, XRT also allows the observed dislocation structure to be correlated directly with device properties.

The important value of the X-situ XRT data already collected has led to the design and construction of a unique combined MBE/XRT chamber. Used in conjunction with the Daresbury Synchrotron, this chamber has already allowed the onset and development of the strain-relaxation process to be monitored in-situ during MBE growth for the first time worldwide. The presentation will describe the important new results which have recently been obtained using the new facility. These unique results are already leading to the development of the first experimentally-verifiable molecular dynamics simulation code for strain-relaxation which will also be briefly described. Finally, an overview of the new experiments now made possible will also be provided.

Acknowledgement

The project described involves formal collaboration between Sheffield, Durham and Hull Universities, DRA Malvern and the SERC Daresbury Laboratory. Continuing project contributions made by A.G. Cullis, S.J. Barnett, G.F. Clark, B.F. Usher, A.M. Keir, A.D. Johnson, B. Lunn, C.J. Hogg, W. Spirkl, J. Jefferson, P. Ashu and Professors B.K Tanner and W.E. Hagston are vital to its success and are gratefully acknowledged.

ENERGY-BAND STRUCTURE OF TYPE I AND TYPE II InGaP/InAlP SHORT PERIOD SUPERLATTICES

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The energy-band structure of two lattice matched InGaP/InAlP short period superlattices (SPSL) grown by metal organic vapour phase epitaxy have been investigated by low temperature photoluminescence (PL) and time resolved PL. These measurements in conjunction with measurements of the direct and indirect band-gaps of a range of InAlP samples and knowledge of the indirect band-gap of InGaP allow the band line-ups in the SPSLs to be determined.

The SPSLs contain 20 repeats of InGaP (thickness, d) with d=10 monolayers (ML) in the first sample and d=8 ML in the second and InAlP with thickness 8 ML for both samples. From the SPSLs' emission energies and their respective life-times it is established that the change in InGaP width from 10 to 8 MLs causes the SPSL to go from a type I band-edge alignment to a staggered type II alignment.

To estimate the conduction-band discontinuity (ΔE_c) and valence-band discontinuity (ΔE_v) in the SPSLs, accurate values for the direct and indirect band-gaps of AlInP are needed. We find, however, that from resonant Raman measurements the room temperature direct gap of partially ordered AlInP samples can vary between 2.50eV to 2.58eV depending upon the degree of ordering and in-built strain. Since the sample with the largest band-gap still showed ordering as indicated from [112] transmission electron diffraction patterns, we estimate that the 4.2K value of the direct band-gap in truly random AlInP must be greater than 2.6eV. In addition we also find that the energy of the lowest X-states in AlInP measured from low temperature PL can also vary by some 20meV. These effects combine to make it difficult to obtain an accurate value of ΔE_c.

Nevertheless, taking the above effects into account we are able to determine ΔE_v to be 0.240±0.04eV and ΔE_c to be 0.340 ± 0.06 eV and that the lowest X-states in the InGaP lie some 175±40meV above those in the AlInP.

Low resistance ohmic contacts to GaAs using Ion Assisted Deposition.

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An ion assisted deposition technique has been developed to produce superior ohmic contacts. This novel technique uses electron beam evaporation to vaporise and partly ionise the contact metallisation. The ionised fraction is accelerated by a negatively biased substrate and implanted into the near surface region of the semiconductor. This has the effect of dispersing the native surface oxide and encouraging intermixing of the contact metal and the semiconductor, allowing a more uniform contact to be formed at lower annealing temperatures.

Contacts were fabricated on degenerately doped (N_d=2x10^{18}cm^{-3}) *n*-type GaAs using a AuGe eutectic, with a Ni overlayer deposited *in-situ* by conventional thermal evaporation. Four samples of varying doses were fabricated and annealed at temperatures up to 500°C. Measurements on TLM test patterns gave contact resistances of approximately 5x10$^{-7}\Omega$-cm^2 for the samples with the higher doses which were annealed at 450°C. This was nearly an order of magnitude lower than the conventional un-ionised sample. The contacts also required less annealing to become ohmic. Above 450°C, the surface of the un-ionised sample began to 'ball up' but the surface morphology of the ionised samples remained laterally homogenous.

To establish the mechanisms that are responsible for lowering the contact resistance, a further two samples were formed on lightly doped (N_d=2x10^{16}cm^{-3}) *n*-type GaAs, epitaxially grown by MBE on a highly doped substrate. Using DLTS analysis, the dominant defect induced in the GaAs using this ionisation process was found with an activation energy of 0.22eV. This damage could be entirely removed after annealing for 1min at 350°C.

As deposited current-voltage-temperature measurements revealed that the ion implantation had caused damage to the near surface region of the semiconductor, leading to a lower Schottky barrier height. After annealing at 300°C, thermionic field emission became the dominant current transport mechanism, with the ionised sample exhibiting a substantially lower barrier height than the conventional sample (0.34eV compared to 0.65eV). The barrier lowering is due to higher n^+ surface doping caused by the premixing of the metal with the semiconductor, together with defect enhanced in-diffusion of the contact metal, leading to ohmic behaviour at lower anneal temperature. It is believed that the lower contact resistance that was obtained at 450°C is due to an increase in the effective area of electrical contact caused by the dispersion of the native oxide.

Fabrication of submicron gratings for 1.55μm DFB lasers using DRYDEL process

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Cork.

Abstract

A process to fabricate submicron gratings has been developed. Application of the DRYDEL process to e-beam lithography and also the inclusion of a thin intermediate layer of SiO_2 to seperate the resist from secondary electrons has enabled high quality gratings (0.12μm lines with 0.24μm period) to be fabricated at 30keV electron beam exposure energy. The work concentrated on the recently introduced Plasmask 302 , a DRYDEL optical resist, and is its first application to e-beam lithography.

Introduction

The resolution of e-beam nanolithography is limited by scattering of electrons in the resist and in the substrate. High energy beams ≥30keV and thin resists can reduce beam broadening in the resist to ≤1nm.[1] Electrons scattered from the substrate are a primary factor in limiting the resolution and are much more dificult to counteract. Three approaches have been used to reduce the effect of electron scattering from the substrate. The standard approach is to use a very high electron beam energy ≥50keV.[2] In this case the electrons penetrate deep into the substrate and elastically backscatter over an area of order of magnitude greater than that of the primary beam. An alternative method but much more recent and still under development is to use a very low energy beam so that the electrons scatter over short distances.[3] The third and also recently introduced is to use a thin SiO_2 intermediate layer to seperate the resist from secondary electrons.[4] In this work the DRYDEL process is used in conjunction with a thin intermediate layer to achieve high resolution gratings while using an e-beam energy of just 30keV. The DRYDEL process transforms the latent optical image into a latent silicon containing image. The resist is exposed to gaseous HMDS ($SICL_4$) whereby silicon is selectively incorporated into the resist regions that have been exposed. The silicon image is subsequently used to produce a relief image by dry etching in oxygen. The silicon containing parts form a SiO_2 rich layer which stops further erosion while other regions are etched away.[5] The latent silicon image is formed on the surface of the resist so the overall effect of backscattering is considerably reduced.

Procedure

A SiO_2 layer 200nm thick was sputtered on the substrate prior to resist spinning. The Plasmask 302 resist was thinned and spun on to a thickness of 0.25μm. This was soft baked for 30 minutes at 90°C.
The electron beam lithography was performed by a Cambridge Instruments EBMF 2-150 machine at 30keV. The exposure dose was 100μC/cm^2 at a clock of 4MHz. The spot sise was 67nm. Following e-beam exposure a blanket near ultraviolet exposure was performed at 50mJ/cm^2.
The samples were then silylalated. First a presilylation bake for 20secs at 205°C. The samples were then baked again for 50secs at 205°C. with HMDS flowing over the resist at 2.5Litres/min.

The samples were then dry developed in an oxygen plasma creating the silicon relief image. To ensure the pattern could be transferred to the SiO_2 layer the samples were exposed in deep ultraviolet for 30mins. Finally the samples were etched in a CHF_3/Argon dry etch .

References

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4. K.W. Rhee, D.I. Ma, M.C. Peckerar, R.A. Ghanbari, H.I. Smith, J. Vac. Sci. Technol. B 10(6), Nov/Dec 1992
5. J. Pike, J.Braddell, W.M. Kelly, ESPRIT 2265-DRYDEL, Final Technical Report, Feb. 1991

Figure 1 Scanning Electron Micrograph of grating in resist

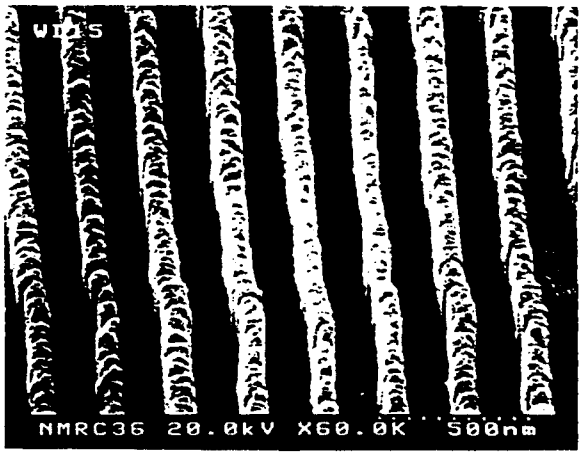

Figure 2. Scanning Electron Micrograph of grating in SiO_2

Session 2: Modelling / Simulation

Chair: E. Kohn (University of Ulm)

1. J.Feng, **D.L.Pulfrey**
   University of British Columbia — Canada
   A physics based, large signal SPICE model for HBTs

2. **J.Schneider**, H.Schumacher
   University of Ulm — Germany
   Self-consistent thermoelectrical model for an AlGaAs/GaAs HBT

3. J.Hedoire, **J.C. de Jaeger**, M.Lefebvre, G.Salmer
   CNRS — France
   2-D hydrodynamic energy model simulation of pseudomorphic HFET: recent results

4. **Mónica Fernández Barciela**, P.J.Tasker, M.Demmler, J.Braunstein, B.Hughes, E.Sánchez
   University de Vigo, Fraunhofer Institute, Hewlett Packard — Spain/Germany/USA
   Novel interactive measurement and analysis system for large signal characterisation of FETS

5. **Vitali I. Yatskevich**
   Technical University of Hamburg — Germany
   Investigation of noise level in GaAs MESFET structures via Monte Carlo simulation

6. **G.J.Rees**, P.B.S. Wong, J.P.R.David, T.W.Lee, P.A.Houston
   University of Sheffield — UK
   Dead space effects in impact ionisation and multiplication

7. O.Abu-Zeid, H.C.Heyker, J.J.M.Kwaspen, **T.G.Van de Roer**, M.Henini
   Eindhoven University and Nottingham University — Netherlands/UK
   Accurate and efficient modelling of double barrier resonant tunneling diodes

8. **N.Cordero**, S.Mackenzie, P.Maaskant, W.M.Kelly
   NMRC — Ireland
   Numerical modelling of GaAs varactors

A physics-based, large-signal SPICE model for HBTs

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A new model for simply, yet accurately, representing heterojunction bipolar transistors (HBTs) in SPICE has been developed. The model is based on the Ebers-Moll formulation of the currents in an HBT [1], and can be implemented in any version of SPICE by invoking the regular macromodel for the homojunction BJT.

The voltage-dependent expressions for the tunneling factor and the abrupt-junction barrier height, which have thwarted previous attempts to simply model the HBT, are taken into account by a new diode ideality factor NF. The derivation of NF will be presented.

The accuracy of the simulation for both DC and large-signal AC conditions will be confirmed by comparing the results from the SPICE model with experimental data. Preliminary comparisons with data from state-of-the-art AlGaAs/GaAs HBTs show excellent agreement under dc conditions and very good agreement under large-signal transient conditions. In the latter case, the comparison was made on the basis of the voltage dependence of the oscillation frequency for a 5-stage ring oscillator. The results suggest a minimum gate delay of 14 ps for a simple RTL stage.

It is believed that this new SPICE model will be of widespread usefulness as it can be so simply implemented in existing versions of SPICE.

1. S.C.M. Ho and D.L. Pulfrey, IEEE Trans. Elec. Dev., **36**, 2173, 1989.

Self-consistent thermoelectrical model for an $Al_{0.3}Ga_{0.7}As/GaAs$ HBT

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The electrical output characteristics of $Al_{0.3}Ga_{0.7}As/GaAs$ power HBTs are degraded due to thermal effects. For example the maximum output power is limited by self-heating, as a consequence of the low thermal conductivity of the $GaAs$ substrate. To improve the electrical output characteristics its important to find thermal design rules, which reduce the maximum operation temperature T_{max} and as a result the self-heating effects. The multilayer and nonplanar structure of such an HBT and the nonlinear thermal behaviour of semiconductors, requires numerical methods to calculate T_{max}.

In this work we numerically investigated an $Al_{0.3}Ga_{0.7}As/GaAs$-HBT with a self-aligned mesa structure and a vertical material layer composition as shown in table 1.

Layer	Material	Doping	Thickness
Metallization	Au		$0.2 - 0.5\,\mu m$
Emitter cap	$GaAs$	$N_d = 5 \cdot 10^{18}\,cm^{-3}$	$0.1\,\mu m$
Emitter	$Al_{0.3}Ga_{0.7}As$	$N_d = 5 \cdot 10^{17}\,cm^{-3}$	$0.2\,\mu m$
Base	$GaAs$	$N_a = 5 \cdot 10^{19}\,cm^{-3}$	$0.1\,\mu m$
Collector	$GaAs$	$N_d = 1 \cdot 10^{16}\,cm^{-3}$	$1.0\,\mu m$
Subcollector	$GaAs$	$N_d = 5 \cdot 10^{18}\,cm^{-3}$	$0.5\,\mu m$
Substrate	$GaAs$	undoped	$100\,\mu m$

Table 1: Material composition of the HBT

To determine the temperature distribution inside such a multilayer structure, one has to solve an eleven-dimensional system of partly nonlinear heat equations

$$-\nabla\left(\lambda_i(T)\,\nabla T(\mathbf{x})\right) = \eta(\mathbf{x},T)\,, \qquad (i = 1,\ldots,11)\,, \tag{1}$$

where $\lambda_i(T)$ denotes the thermal conductivity of the i-th material layer. The source term $\eta(\mathbf{x},T)$ in the equations above, creates the coupling between the thermal and electrical quantities. Assuming a temperature dependent collector current $I_c(T)$, homogeneous distributed inside the intrinsic collector depletion region $V_{ci} = A_e \cdot d_{bc}$, one gets the following expression for the dissipated power density

$$\eta(T) = \frac{U_{bc}(T) \cdot I_c(T)}{A_e \cdot d_{bc}(T)} \;\; \forall \;\; \mathbf{x} \in V_{ci}\,, \tag{2}$$

where U_{bc} is the internal base-collector junction voltage and A_e, d_{bc} describes the emitter area and the depletion-layer width of the base–collector junction respectively. Determinating the electrical characteristics $I_c(T)$ and $U_{bc}(T)$ of the HBT, means to solve simultaneously (1) with the diffusion equation for electrons in the base and the diffusion equation for holes in the emitter and the collector.

At the conference we will present a numerical model, which determines self–consistently the electrical and thermal quantities of the problem described above. To get the temperature distribution of (1), we used a semianalytical method where we solved, in a first step, the ten–dimensional system of heat equations for the mesa–structure with the help of a finite element program. Subsequently we calculated the threedimensional temperature distribution inside the substrate, by linearisizing the heat equation using the Kirchhoff–Transformation

$$\theta(\mathbf{x}) - T_s = \frac{1}{\lambda_s} \int_{T_s}^{T(\mathbf{x})} \lambda(T')\, dT', \quad \lambda_s = \lambda(T_s) \tag{3}$$

and making a separation ansatz for the transformed temperature distribution $\theta(\mathrm{x})$ and a double Fourier series expansion in the lateral x– and y–direction

$$\theta(x,y,z) = \sum_{n,m} c_{nm}(z) \cdot \cos\left(\frac{2\,n\,\pi\,x}{l_x}\right) \cdot \cos\left(\frac{2\,m\,\pi\,y}{l_y}\right) . \tag{4}$$

l_x , l_y : lateral extension of the substrate in the x– and y–direction

Such an semi–analytical approach significiantly cuts down the CPU time and memory requirements.

The electrical quantities were calculated by using an analytical diffusion model for a graded base–emitter junction and an analytical thermionic diffusion model for an abrupt base–emitter junctions. Additionally we considered the temperature dependence of all physical quantities.

Further we will present numerical results showing the temperature dependence of the output characteristics of an $Al_{0.3}Ga_{0.7}As/GaAs$ HBT. We will show the influence of thermal design rules and the influence of heat sinking via metallization contacts on self–heating effects. A comparison between the temperature dependent electrical quantities of an abrupt and graded HBT will also be done.

2D-HYDRODYNAMIC ENERGY MODEL SIMULATION OF PSEUDOMORPHIC HFET : RECENT RESULTS

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The pseudomorphic AlGaAs/InGaAs/GaAs HFET (PMHFET) is the most promising device for power applications in the millimeter wave range (F > 30 Ghz). For the optimization of this structure, a physical simulation is necessary in order to obtain a good understanding of the phenomena which occur due to the device complexity.

In this paper, we propose to study the influence of two main parameters on the performances of power PMHFET :

- the temperature which causes limitations on the microwave performances ;
- the gate-recess shape which constitutes the most important parameter for the study of the breakdown voltage.

The physical study of power structures is analysed using a two-dimensional transient hydrodynamic energy model based upon Poisson's equation and those derived from Boltzmann Transport Equation : the particle, momentum and energy conservation equations [1] [2]. This model takes into account the main physical phenomena which occur in PMHFETs operating at very high frequencies. Moreover, it was validated by a comparison with experimental results.

For the study of the temperature influence, the transport properties of the semiconductors versus the temperature are first determined from Monte Carlo simulations and then introduced in our physical model. The effect is studied for the respective temperatures of 300 K, 400 K and 500 K.The results obtained show that the temperature dependance on the power device performances is very important. It is demonstrated that a small increase of the carrier density N_s in the GaInAs well and also an increase of the pinch-off voltage are observed when the temperature is higher due to the thermic effect. As consequence, the C_{gs} capacitance variations are very small. But, considering the transconductance g_m of the device, a large decrease versus the temperature is noted mainly due to the carrier velocity effect. The maximum transconductance is varying from 1200 mS/mm at T = 300 K to 900 mS/mm at T = 400 K for a 0.15 µm gate lenght δ-doped transistor. The potential performance evolutions are also deduced. For instance, it is shown that a large decrease of the intrinsic current gain cut-off frequency is observed but the variations of the maximum available gain are very low. At 60 GHz it is close to 11 dB at T = 300 K and becomes equal to 9 dB à 500 K.

The gate-recess constitutes also an important parameter for the optimization of power devices. For the introduction of the gate-recess in our two-dimensional model it was necessary to bring important modifications. It is possible to study the influence of the shape and the size of the gate-recess on the main parameters in the structure and to deduce a good behaviour of the physical phenomena which occur. It is demonstrated that in the gate-drain distance, the variations of the potential take place mainly in the recess zone. This phenomenon involves a better potential distribution in the whole structure for larger recess-width and as a consequence a decrease of the electric field which is favourable for the breakdown voltage. The study of the carrier distribution in the transistor and the evolutions versus the gate and drain biases bring interesting informations on the depleted zone shape and the physical behaviour for a gate-recess structure. The influences on the potential device performances are also studied, for instance the intrinsic equivalent scheme.

The informations describe in this paper are very interesting in order to help industrial laboratories to perform the optimization and the development of power PMHFETs. They can also be useful for approach simulations such as quasi two dimensional models.

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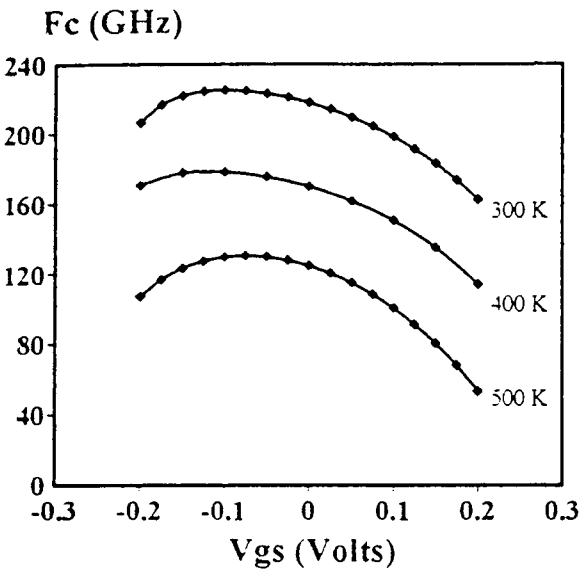

Fig. 1 : Influence of the temperature on the intrinsic current-gain cut-off frequency (single δ-doped PMHFET $\delta = 3x10^{12}$ cm^{-2} ; $l_g = 0.15$ µm ; $V_{ds} = 3$ V).

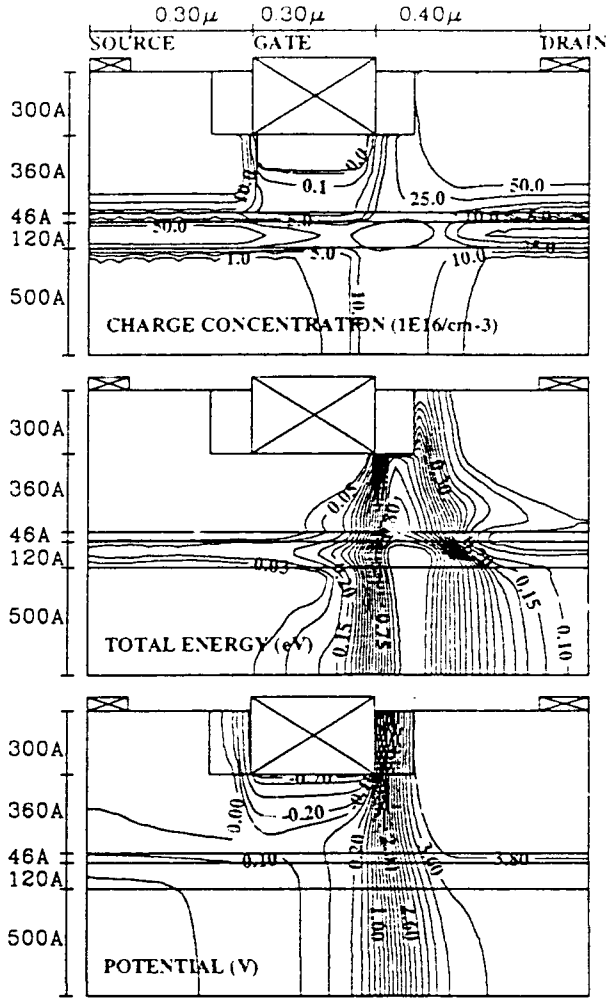

Fig. 2 : Distribution of physical quantities in a PMHFET gate-recess device (R = 0.1 µm ; $V_{gs} = 0V$; $V_{ds} = 4V$).

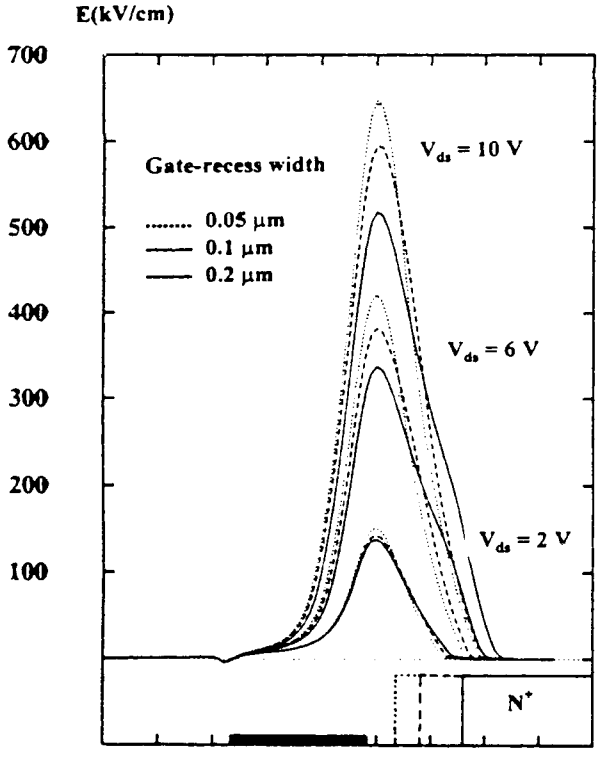

Fig. 3 : Average electric field in the channel for a gate-recess PMHFET. Influence of the gate-recess width for different biases V_{ds}.

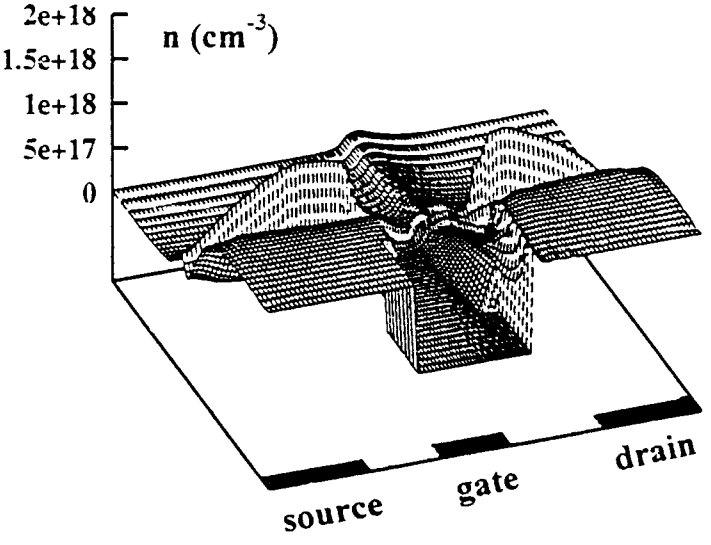

Fig. 4 : Evolution of the charge concentration in a gate-recess PMHFET (R = 0.1 µm ; $V_{gs} = 0$ V ; $V_{ds} = 4$ V).

Novel Interactive Measurement and Analysis System for Large Signal Characterisation of FETs

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Abstract

A novel interactive and fully integrated data acquisition and analysis system has been developed for Large Signal Characterisation of transistors. This system makes direct use of the novel S-parameter measurement concept: S-parameter "Bias Scans" in which S-parameters are measured in "real time" as a function of bias rather than frequency. Analysis of this data allows for both "real time" extraction and "on line" analysis of the large signal constitutive relations required to model the non-linear behaviour of transistors, i.e., the Gate and Drain currents and charges as a function of Gate and Drain Bias Potentials. "On line" analysis of the extracted parameters, for example, using different integration paths allows quick determination of device characteristics and checking of model assumptions, and so is a valuable tool for determining accuracy in model generation.

Introduction

Look-up-table device models have demonstrated their usefulness as a CAD tool for large signal analysis and design. In these *Table-based* or *Spline based* empirical device models [1] the transistor is characterised at each terminal by means of a set of (non-linear) algebraic constitutive relations (I,Q), defined in terms of the controlling voltages (V_G,V_D). The circuit simulator is then able to use these sets through multidimensional spline interpolation. The problem with these models is that they require a very time consuming and detailed device characterisation in order to obtain an accurate large signal device model.

Measurement System and Model Implementation

An *interactive data acquisition* and *analysis* system based on a conventional on-wafer small signal S-parameter measurement system, controlled by a special software package has been developed for large signal characterisation of transistors. This system utilises the novel S-parameter measurement concept: S-parameter "Bias Scans"[2]. S-parameter "***Gate Bias Scans***" or "***Drain Bias Scans***", for example, are obtained when an error corrected Network Analyser is configured to perform, in "real time", S-parameter measurements as a function of Gate Potential or Drain Potential respectively rather than frequency. Figure 1, shows the configuration. The software package developed exploits the fact that this data, along with the appropriate DC measurements, is all that is required for both "real time" extraction and "on line" analysis of the *large signal constitutive relations* needed to model the **non-linear behaviour** of transistors. In addition, it is possible to perform the extraction of the constitutive relations using two different integration paths and different boundary conditions. An important objective of this approach was to provide an *interactive* tool for large signal model development and *verification*.

Based on this measurement data a lookup table model has been developed for large signal device simulation in the framework of the commercially available software package Microwave Design System from Hewlett Packard. The non-linear model used in this case follows closely Root model approach, however, it is based on Symbolically Defined Devices (SDD). Figure 2, shows as an example the current gate constitutive relations generated for this model using the measurement and characterisation system proposed.

Validation of Modelling Concepts

Key features of large signal models have been investigated using this model. First, an *extrinsic* version of the model using current constitutive functions extracted only from *DC data* has been used to simulate the power performance of MODFET devices in the frequency range required for mobile communications, around 2GHz. Figure 3, shows the excellent agreement obtained with this simplified model between measured and simulated output power levels up to 4th harmonic (8 GHz). This result confirms the relatively small low frequency dispersion phenomena measured in these devices. These effects can therefore be neglected in this case, allowing model simplification. Secondly, we have investigated the validity of one of the main assumptions in the model: the path independent contour integral assumption needed to generate an unique set of constitutive relations. For this purpose the constitutive relations were determined from a set of measured drain bias scans and then the model was used to simulate a set of gate bias scan. The comparison between modelled and measured extrinsic Y parameters is presented in figure 4, which shows the simulated an

measured real part of Y_{21}. As a consequence of the validity of the path independent assumption for these devices the results shows that it has been possible to model the transconductance (Y_{21}) and input (Y_{11}) non-linear behaviour from only the measured output conductance (Y_{22}) and feedback (Y_{12}) behaviour.

Conclusions

A novel ***interactive*** and ***fully integrated measurement*** and *analysis* system has been developed for *Large Signal Characterisation* of transistors. This system performs in "real time" the measurement and analysis of bias dependent S-parameters measurements for large signal parameter extraction. The interactive nature of this tool allows a quick check of device characteristics and model validation and reduces the time required to develop and extract non-linear device models. The system has been successfully used to generate a non-linear CAD model for simulating the large signal behaviour of MODFET transistors.

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Acknowledgements

The authors would like to thank the technology group of the Fraunhofer Institute for HEMT processing and M. Schlechtweg at Fraunhofer Institute and D. E. Root at Hewlett Packard for their cooperation and valuable discussions. This work was supported in part by the University of Vigo, Spain.

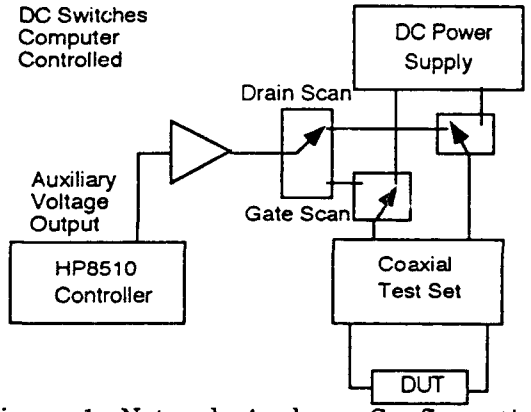

Figure 1. Network Analyser Configuration required for "Bias Scan" S-parameter Measurements.

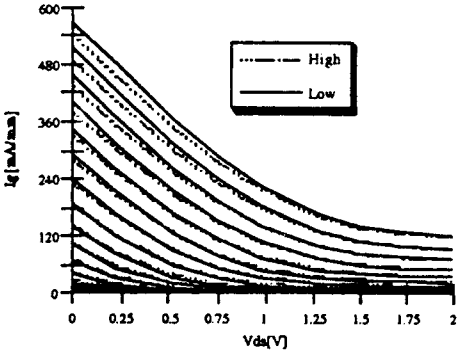

Figure 2. Extrinsic Current Constitutive relations ($I_{low;G}$ and $I_{high;G}$ following Root notation) at gate terminal for a 0.15x100 μm^2 pseudomorphic MODFET extracted from a sequence of Gate Scan measurements performed at 2 GHz. In this case very little dispersion between relations generated using DC or RF data is observed

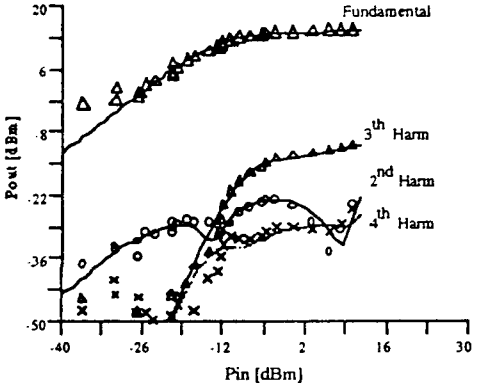

Figure 3. On-Wafer Measured (symbols) and Simulated (lines) fundamental (2GHz), second (4 GHz), third (6 GHz) and fourth (8 GHz) harmonic levels (dBm) vs. Input power for a 0.6x100 μm^2 pseudomorphic MODFET. Bias V=-0.6. The model uses current constitutive functions extracted only from DC data.

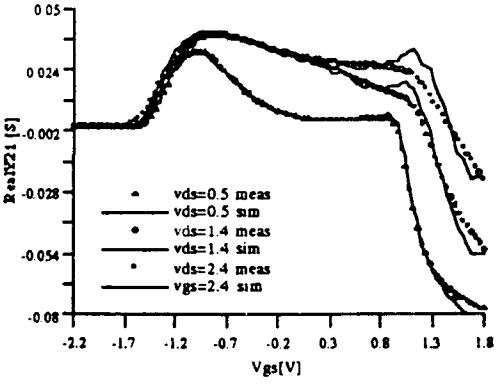

Figure 4. Extrinsic real part of (Y_{21}) vs. gate voltage measured and modelled on a 0.6x100 $\mu m2$ pseudomorphic MODFET using extrinsic "Drain Bias scans" to generate the model.

INVESTIGATION OF NOISE LEVEL IN GaAs MESFET STRUCTURES VIA MONTE CARLO SIMULATION

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Monte Carlo simulation represents one of the fast-growing and perspective methods for the computer-aided modelling of semiconductor devices and integrated circuits. The description of physical processes which is effectively incorporated in the model enables one to determine the parameters of a semiconductor device at the early stage of design.

Noise factor belongs to the most important parameters which determine the efficiency of an amplifying semiconductor element. The numerical methods used in the past to compute the atorementioned parameter appear to be rather complicated in the numerical respect and pose severe requirements as to the computer storage and speed of computations [C.Jacoboni, P.Lugli, The Monte Carlo Method for Semiconductor Devices Simulation, New York, Springer, 1989].

In the present report, a novel efficient method for the noise factor calculation is proposed which is based on the Monte Carlo simulation and which exploits the relationship between the noise factor and the noise temperature, the latter being the measure of the mean noise level. An explicit expression for the noise temperature is derived which utilizes the assumptions of the Maxwellian distribution for the electron velocity and accounts for the existence of a non-equilibrium state due to the difference between the electrons' and the crystall grate temperatures. In addition, the ergodic character of the collective statistical parameters of the electron gas in a semiconducting material ín presence of the external electric field is presumed. A computer code has been developed implementing the above described theoretical model, and the extensive numerical analysis of noise level in GaAs MESFET structures has been carried out. In the report, the results of these investigations are discussed and some practical recommendations are formulated.

Dead Space effects in Impact Ionisation and Multiplication

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Carrier multiplication due to Impact Ionisation (II) is normally modelled assuming a local dependence on electric field of α and β, the II coefficients for electrons and holes. While the effects of carrier acceleration and soft threshold are well understood to lead to a 'dead space' in which $\alpha(x)$ and $\beta(x)$ depend on position, rising to their equilibrium values as the carriers gain energy from the electric field, this non-local effect is normally only included in a rudimentary manner for the first carrier[1], or not at all[2]. In fact each extra pair of carriers produced by an II event are generated 'cool' and must acquire threshold energy by accelerating in the field prior to impact ionising again. Thus a satisfactory model for multiplication should allow for non-local II throughout the multiplication process.

In this paper we report a method for modelling multiplication in uniform fields which accounts for non-local effects at each II event. Our technique considers local multiplication rates for electrons and holes whose dependence on position obeys coupled integral equations with kernels which depend in turn on $\alpha(x)$ and $\beta(x)$. These equations are easily solved using standard numerical techniques and their solutions can then be integrated to yield M_e and M_h, the multiplication coefficients for pure electron and hole injection. Our results agree with the more simply derived conventional expressions[2] when the appropriate local approximations are made to α and β.

We also report measurements of multiplication of photogenerated electrons and holes in GaAs pin diodes. Our measurements show values of excess multiplication, M_e-1 and M_h-1, around a factor of two higher than those calculated from published[1] data for α and β using the conventional local model for II. We demonstrate the effect of including non-local behaviour on such calculated multiplication curves. Using a simple model which assumes a ballistic dead space and initially cold carriers we interpret our measurements to deduce equilibrium values for α and β which exceed published values by 30% or more.

Acknowledgement

Part of this work was supported by DRA, Malvern.

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ACCURATE AND EFFICIENT MODELING OF DOUBLE BARRIER RESONANT TUNNELING DIODES

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Abstract

Double Barrier Resonant Tunneling diodes have been investigated experimentally with respect to their d.c. characteristics and microwave impedance and noise properties. A theoretical model has been developed to account for the measured data.

In the model account has been taken of the contact regions. It is found that the 2D character of electrons in the injection region has a significant influence on the I-V curve. Incoherent tunneling has been accounted for by a simple scattering model. Altogether the measured I-V characteristic can be reproduced accurately.

A microwave noise model has been made on the assumption that shot noise is the main noise source and taking into account the feedback caused by the space charge in the quantum well. It predicts a reduction of the noise, compared to full shot noise, in the regions of positive differential resistance and an increase in the negative-resistance region. These predictions are confirmed by measurements at 1.5 GHz.

Microwave impedance measurements up to 18 GHz can be represented very well by an equivalent circuit consisting of the d.c. differential resistance in parallel with a voltage-dependent capacitance. The latter shows a sharp peak in the region of negative differential conductance. This too is predicted by the model.

Numerical Modelling of GaAs Varactors

N. Cordero, S. Mackenzie, P. Maaskant and W.M. Kelly

ABSTRACT

A varactor, or nonlinear voltage-controlled capacitor, is a critical element of most harmonic multipliers for submillimetre-wave receivers. The typical varactor is a GaAs Schottky barrier diode[1]. As the operating frequency increases, the device capacitance must decrease which is accomplished by reducing the device area[2].

To improve the efficiency of the varactor at low input power, the nonlinearity of the C-V characteristic must be increased. A novel structure is the BNN (Barrier-n-n^+) varactor, in which combinations of depletion layer dopings and planar doping sheets (Fig. 1) allow tailoring of the C-V characteristics. The BNN structure gives a greater capacitance modulation than conventional Schottky barrier varactors.

Due to the complexity of the BNN varactors, simulation tools are required for their design. Analytical (closed form) models are widely used in Schottky diode simulation. However, they are useful only for uniformly doped structures. One dimensional (1-D) numerical models under-estimate diode capacitance since they don't include edge effects. Therefore, to accurately model BNN varactors, a full 2-D numerical model is required.

Our model is based on an in-house simulator developed for GaAs MESFETs[3]. The modelled BNN varactors have circular contacts, therefore the program was modified to take into account cylindrical coordinates.

The structure on fig. 1 was modelled using this program. The modelled and experimental results are shown on fig. 2. There is a very good agreement between theory and experiment. The main characteristics of this device are a $C_0 \approx 25$ fF and a capacitance swing (C_{max}/C_0) around 2.5.

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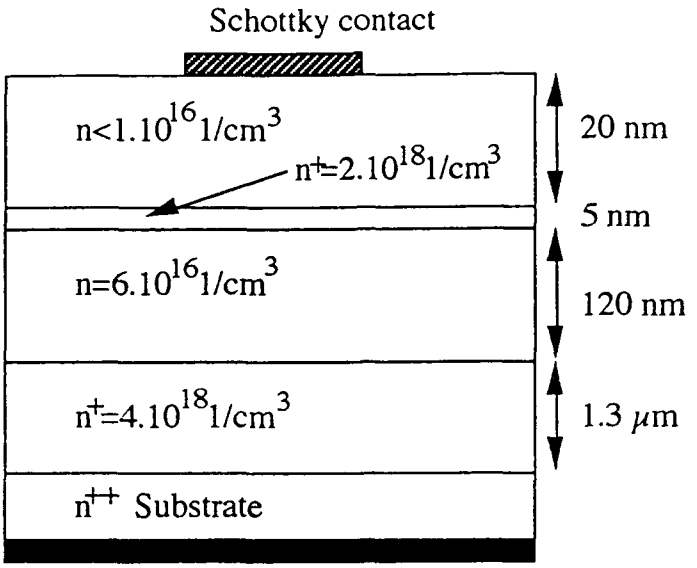

Figure 1. BNN GaAs Varactor

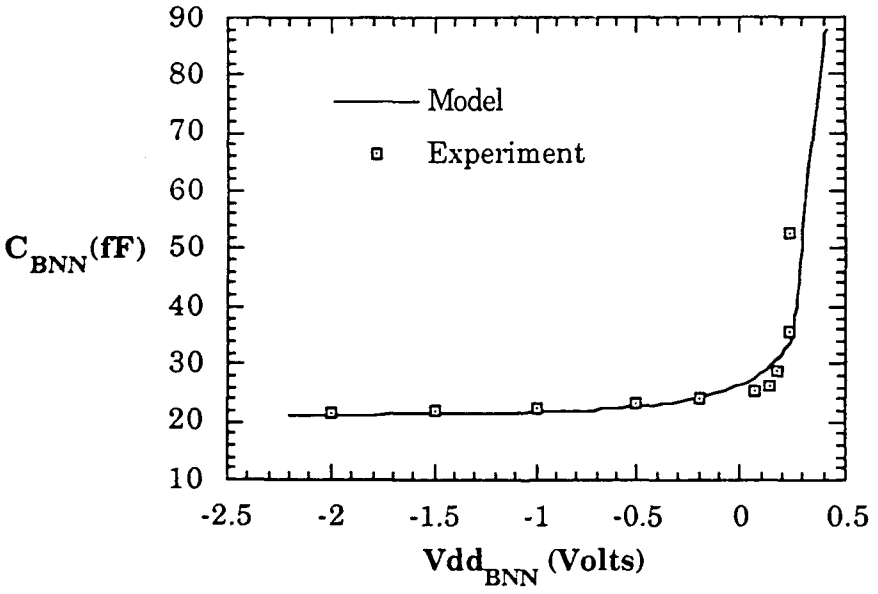

Fig. 2. Measured and calculated C-V characteristic for GaAs varactor

Session 3: Transistors 1:

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1. **M.Berroth** (Invited)
   Fraunfofer Institute — Germany
   III/V High speed circuits

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   University of Ulm, IEMN — Germany/France
   LT-GaAs MISFET small signal characteristics

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    CSELT — Italy
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III-V High Speed Circuits

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During the last years GaAs MESFETs have become a major challenge for silicon integrated circuits in the high frequency range. Analog integrated circuits at microwave frequencies are dominated by GaAs circuits. The advantage of higher transit frequencies has to be accompanied by large scale integration for digital applications. About one million MESFETs are now integrated on the most complex GaAs digital circuits.

Even higher transit frequencies are available with pseudomorphic heterostructure field effect transistors. Several research labs have fabricated those HEMTs with transit frequencies beyond 150 GHz. Now analog integrated circuits are arising for applications up to and even beyond 100 GHz. The IAF has fabricated amplifiers up to 80 GHz using coplanar matching networks. Oscillators and mixers are under development using the same technology for future single chip receivers in the millimetre wave frequency range.
The pseudomorphic HEMT devices are also investigated for digital circuits with gate lengths below 0.3 µm. Excellent threshold uniformity due to molecular beam epitaxy and dry recess etch promises very high integration densities for digital circuits with GHz clock rates. The IAF has demonstrated dynamic frequency dividers using pseudomorphic HEMTs for input frequencies beyond 50 GHz.
High speed and high precision is required for analog-to-digital converters as well as digital-to-analog-converters with sampling rates of more than two billions per second. A resolution up to eight bits can be expected using low power direct coupled FET logic on a single chip converter.
Very large interest is on the development of integrated circuits for high speed optical links. Beside analog functions like laser driver or transimpedance amplifier also digital ICs like multiplexer and demultiplexer are required. The IAF is developing a chip set for 20 Gbit/s optical link whose most advanced components are already indicating functionality at this data rate. An additional advantage of GaAs is the monolithic integration of optical emitters and detectors with high speed electronic circuits. The IAF has demonstrated both, monlithic transmitter and receiver, optoelectronic integrated circuits for Gbit/s transmission links.

LT-GaAs MISFET Small Signal Characteristics

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Abstract

MISFETs with LT-GaAs as the insulator have been developed primarily for power applications. They operate in the deep depletion mode, where the high GaAs interface state density is kept in equilibrium by a controlled leakage current [1]. This leakage current is also present between gate and drain, however negligible in comparison to the open channel current. It will influence the static field distribution and therefore also the bias point dependent small signal characteristics especially concerning the feed back parameters.

Near pinch-off, the surface leakage will smooth out the lateral field and part of the donor charge in the channel may partially be vertically neutralized [2], thus the high field drift region can extend further. At high current, the lateral field will mainly be reduced at the gate edge, thus reducing the stability of the stationary high field Gunn-domain.

Both phemomena were investigated on (planar) LT-GaAs MISFETs grown by MBE with 80nm LT-GaAs lossy gate dielectric and 20nm AlAs diffusion barrier. Gate length was 1µm and the doping thickness product $N_Dt=2.5x10^{12}cm^{-2}$. The DC MISFET output characteristics (fig.1) shows a maximum saturated current (at $V_G=+1V$) of $I_{Dmax}=320mA/mm$ and a maximum g_{mdc} of 63mS/mm. In saturation ($V_D>3V$) at medium current levels a NDR-regime is seen, which is also present at microwave frequencies with $|S_{22}|>1$ (fig.3). Thus, the NDR-region is not of thermal origin. Fig.2a shows the MSG/MAG and H_{21} gain curves at the optimum f_T bias point ($V_D=2.0V$; $V_G=-3.0V$), resulting in a $f_{T(H21)}=8.5$ GHz, and $f_{max(MAG)}=44GHz$. The equivalent circuit analysis is shown in fig.2b. A standard equivalent circuit model can be fitted. Thus, in the GHz regime the input and feed back losses can be neglected. The analysis reveals, that f_T is dominated by a parasitic layout related capcitance. The intrinsic f_{T0} is 14.5GHz, which translates into $f_{T0}L_g=1.2x10^7cm/s$, an effective velocity characteristic of collision dominated transport in a wide drift region. This is consistent with a low C_{gd} and high f_{max}.

The f_{max} obtained at the optimum f_T bias point is unusually high for a 1µm-gatelength GaAs device and such data have only been reported in the InGaAs/InAlAs heterostructure materials system on InP or methamorphic on GaAs [3]. Although a number of parasitic effects enter into the f_T/f_{max} formula, it can be seen that a small $C_{gd}=6.6fF$ and the high ratio $C_{gs}/C_{gd(Vds=2V)}=7.9$ are mainly responsible. A small C_{gd} can be asscociated with a small drift domain capacitance and long lateral drift domain, again consistent with the current understanding.

To simulate the LT-GaAs surface layer conditions, in a first attempt the LT-GaAs was modeled by an undoped GaAs layer. This will ignore the deep donor conduction band conductivity. However, in the case of no current flow, electrostaticially the influence of the conductivity was taken into account by an imposed linear lateral surface potential distribution between gate and drain. Indeed, near pinch-off an essentially extended drift region is seen and at high current levels Gunn-domain formation is predicted. Both results support the experimental findings. However, further analysis is needed to understand the phenomena involved in detail.

Acknowlegement and References

This work was supported by the CEC ESPRIT Basic Research Action 6849 TAMPFETS

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Figures

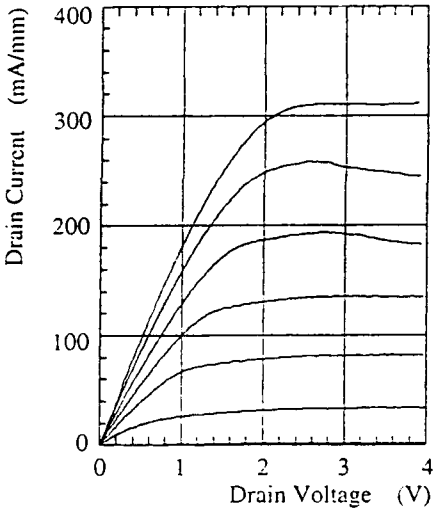

Figure 1: DC-Outpucharacteristic

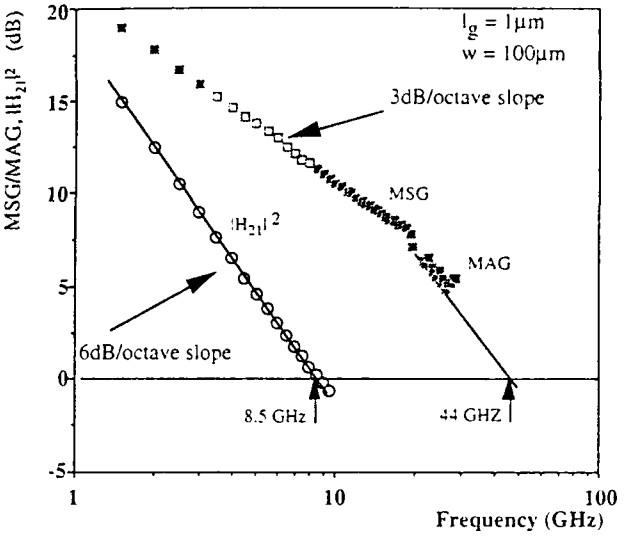

Figure 2a: MSG/MAG and H_{21} at the optimum bias point (V_D = 2V, V_G = -3V)

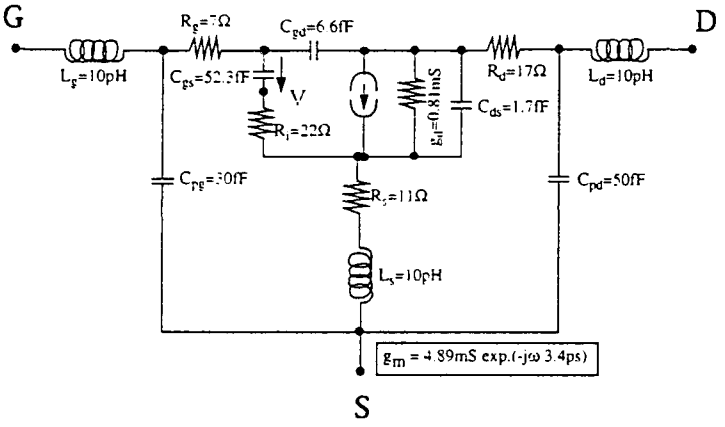

Figure 2b: Fitted standard FET equivalent circuit

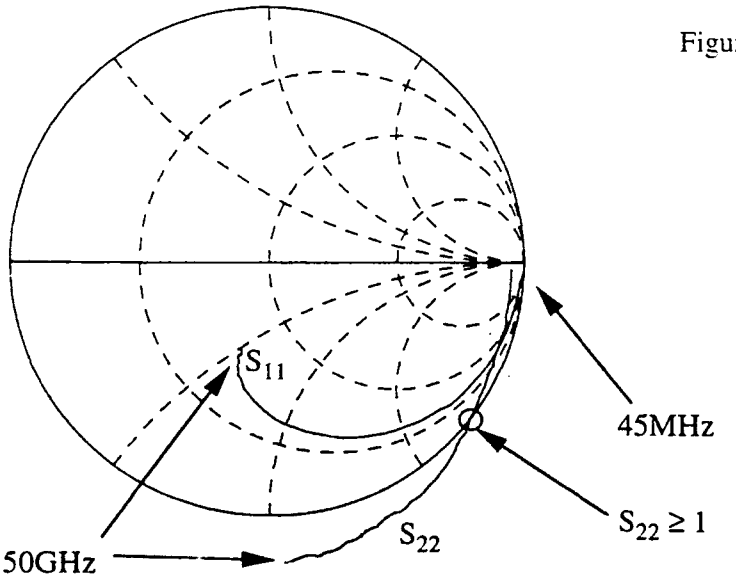

Figure3: Smith-Diagram showing S_{11} and S_{22}>1

The Characteristics of a GaAs MISFET with a low-temperature grown GaAs insulator

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Low temperature (LT) MBE-GaAs has attracted much attention. The annealed LT-GaAs has been used as buffer and insulator to reduce the side-gate effect[1] and to improve the breakdown voltage[2] of GaAs MESFETs and MISFETs. Although the application of the LT-GaAs in MISFETs has been successful, the breakdown voltage is seen to decrease rapidly as the temperature T, was decreased. A transient behaviour of FET's output and a frequency dispersion of transconductance have been observed, and attributed to the existence of a high density of defects. On the other hand, GaAs-MISFETs with as-grown LT-GaAs insulator have shown a record high power with an increase of breakdown voltage on cooling[3]. In this paper, we report a systematic characterization of this type of MISFET.

The LT-GaAs MISFET contains a 5000Å undoped buffer layer, a 500~1000Å active layer doped to $5x10^{17}$-$2x10^{18}cm^{-3}$ with Si, a diffusion barrier and a 800Å LT-GaAs layer grown at 200°C. AuNiGe was used to form Ohmic contacts with overlapping and non-overlapping configurations. A parallel investigation was carried out on the LT-GaAs (1μm on SI-GaAs) planar structure.

1. The formation of the LT-GaAs on the n^+-GaAs active layer leads to a high saturation current I_{DS}, in the range 600~900mA/mm, and a transconductance of 130~160mS/mm, comparable to the conventional GaAs-FET. MISFET showed a good pinch-off and well saturated characteristics, and can be operated at forward bias even at V_F=2V without excessive leakage current. As-grown LT-GaAs MISFETs showed insensitivity to light and no obvious hysterisis of I_{DS}, whereas light sensitivity and a large hysterisis of I_{DS} was observed from MISFET with non-overlapping structure and annealed LT-GaAs insulator.

2. The breakdown voltage V_{BD}, for the gate-drain contact is typically 40~60V for a spacing of 2μm, (defined by 1mA/mm current level), much higher than that of a conventional FET with a similar doping. V_{BD} was observed to increase with decreasing temperature, and the reverse current before breakdown was ohmic. The reverse gate current at a fixed bias decreases slowly on cooling with an activation energy of E_A=0.1~0.2eV, while that of a MISFET with an annealed LT-GaAs showed a value of E_A=0.6~0.7eV. The low value of E_A ensures a high value of V_{BD} and power at low temperature without freeze-out, similar behaviour is expected at high frequency domain.

3. A gate lag effect measurement showed that no transient behaviour was observed from the drain-source output of the MISFET with as-grown LT-GaAs, whereas large gate and drain lag effects were observed from MISFETs with annealed LT-GaAs insulator and non-overlapping structures. The transconductance showed no obvious frequency dispersion for as-grown LT-GaAs MISFET, but a large frequency dispersion for MISFET with annealed LT-GaAs insulator and non-overlapping structure.

The characterization of the LT-GaAs suggested that as-grown LT-GaAs is responsible for the superior properties of LT-GaAs MISFETs: 1. the LT-GaAs passivates the n^+-GaAs surface, eliminating surface state related phenomena. 2. a high defect density provides a high degree of hopping conduction in the as-grown LT-GaAs layer, leading to Ohmic conduction and a consequent uniform distribution of electric field, which avoids the premature breakdown at the surface and other non-uniform space charge effects. 3. the high breakdown voltage of the LT-GaAs is preserved in the MISFET

Thermal annealing at >500°C however, causes the precipitation of arsenic in As-clusters, though the high breakdown voltage is maintained. Since the release of the trapped electrons from clusters is a thermally activated process, it accounts for the transient behaviour, the lag effect and high activation energy of the reverse current of the MISFET with annealed LT-GaAs and non-overlapping structure.

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Temperature Dependence of Current Gain in High C-doped Base HBTs

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Abstract: AlGaAs/GaAs HBTs are the most wildly investigated and have demonstrated excellent RF performance. However, this structure has many well known disadvantages. An alternative to this structue is to use the aluminium-free InGaP/GaAs HBTs which is lattice matched to GaAs substrates. This structure has recently attracted considerable attention due to the favourable energy band line-up properties. Recently we have reported high C-doped base InGaP/GaAs HBTs with improved characteristics showing current gain greater than unity at very low collector current [1]. We have also reported the temperature dependence of current gain on InGaP/GaAs and AlGaAs/GaAs HBTs and showed that the current gain of InGaP HBTs is insensitive to temperature [2]. The temperature dependence of current gain of these devices has not yet been fully understood. Although there have been several reports on the temperature dependence of current gain of HBTs there are no adequate explanation as to what causes the current gain to degrade with increasing temperature.

In this paper we present results detailing the cause of current gain degradation with temperature. The current gain of several single heterojunction HBTs based on AlGaAs/GaAs and InGaP/GaAs materials was measured from 300K up to 600K. Figure 1 shows the normalised current gains as a function of temperature for several high C-doped base HBTs having similar fabrication steps. It is seen that the base ideality factor has a significant effect on current gain stability with temperature. Since near ideal I-V characteristics can be achieved readily in InGaP/GaAs, devices utilising InGaP showed insensitive current gain with temperature. This characteristic makes this material system a very attractive candidate for analogue integrated circuit applications.

In addition, it is shown that devices with a base current dominated by base bulk recombination (devices with base doping $>1x10^{19}cm^{-3}$) have near constant current gain with temperature. In contrast, devices with surface or emitter/base space-charge recombination (devices A and EET-A which has an emitter etched design structure) show a decrease in current gain with temperature. These results show the importance of improving growth processing to minimise space-charge and surface recombination currents.

We have also investigated the quality of the $In_{0.5}Ga_{0.5}P$ material and compare this with $Al_{0.3}Ga_{0.7}As$ by DLTS measurements on emitter/base heterojunction of two HBTs, one with InGaP emitter and the other with AlGaAs. These results will also be discussed.

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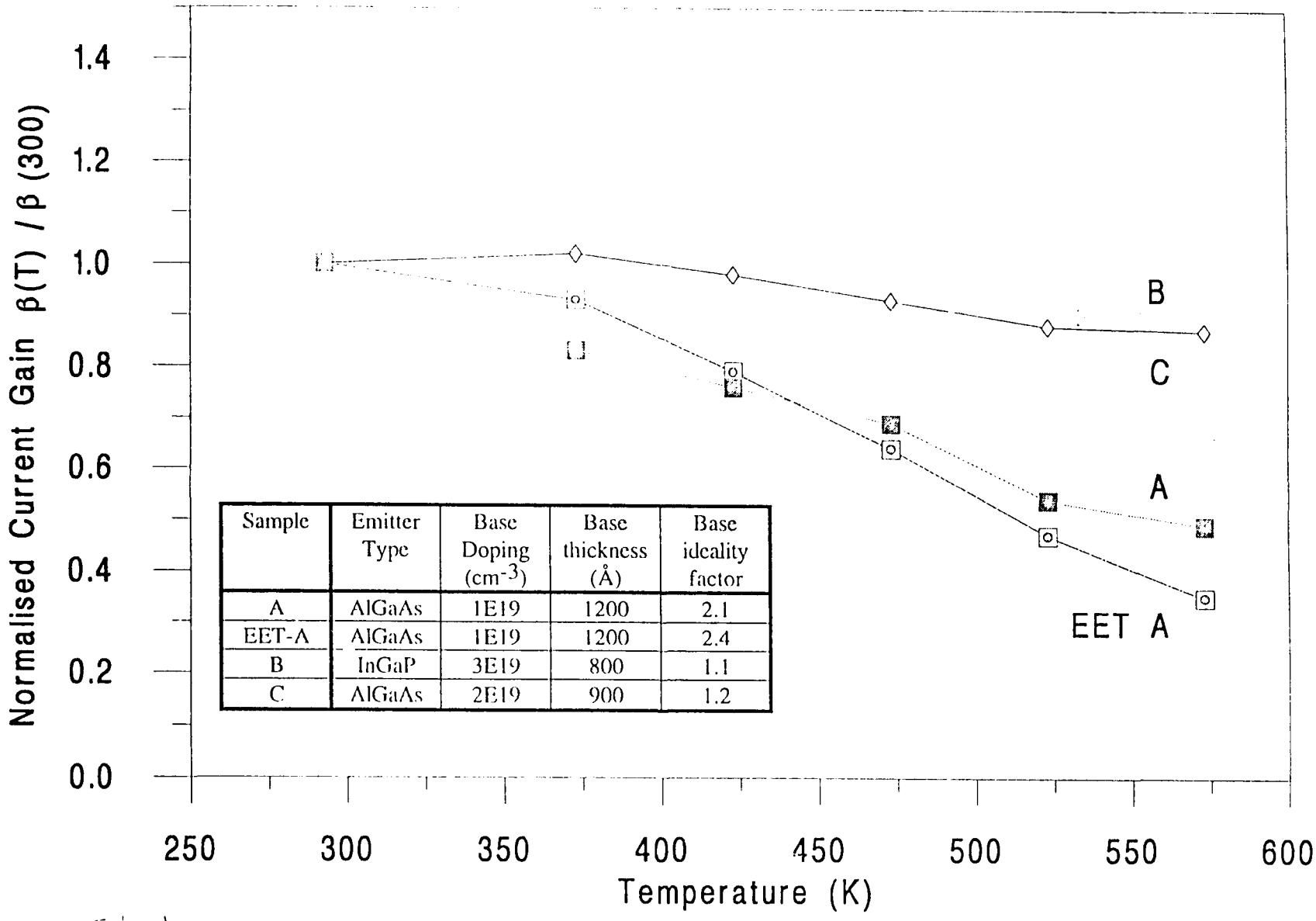

Sample	Emitter Type	Base Doping (cm^{-3})	Base thickness (Å)	Base ideality factor
A	AlGaAs	1E19	1200	2.1
EET-A	AlGaAs	1E19	1200	2.4
B	InGaP	3E19	800	1.1
C	AlGaAs	2E19	900	1.2

Transistor properties of focused-ion-beam defined in-plane-gated channels in $GaAs/In_{0.1}Ga_{0.9}As/Al_{0.2}Ga_{0.8}As$ heterostructures

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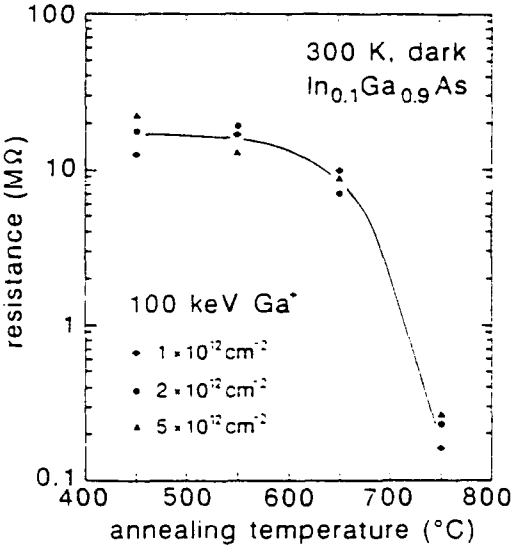
In-plane-gated (IPG) field-effect transistors in $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructures are one-dimensional inherently self-aligned sub-micron devices working at room temperature. The use of $GaAs/In_xGa_{1-x}As/Al_{0.2}Ga_{0.8}As$ heterostructures where the electron gas is contained in a strained $In_xGa_{1-x}As$ layer has already drastically improved the performance of in-plane-gated transistors fabricated by focused ion beam (FIB) implantation of 100 keV Ga^+ ions (A.D. Wieck and K. Ploog, Appl.Phys.Lett. 61, 1048 (1992)). We have investigated the isolation properties of FIB-written lines in $In_{0.1}Ga_{0.9}As$.

Excellent isolation is obtained over a wide range of ion doses. The isolation is not reduced significantly by a post-implantation annealing process up to 550 °C. Between 650 °C and 750 °C, relaxation or interdiffusion of the heterostructure layers is initiated, which destroys the confinement of the 2DEG.

The low ($\approx 10^{12}\,cm^{-2}$) ion dose necessary to obtain isolation allows a very fast structuring. The time for writing 10 μm is well below 1 ms, thus rendering the implantation process insensitive to 50 Hz noise and low-frequency mechanical vibrations which are difficult to damp.



We have measured the $In_{0.1}Ga_{0.9}As$ IPG transistor drain currents in dependence on the ion implantation dose and the annealing temperature. The standard deviations in the saturation currents are 10–20 μA, which corresponds to a 5–10 % (50–100 nm) deviation in channel width. Channels which are defined by a higher dose are less conductive due to side dose. Contrary to the case of $GaAs/A_{0.3}Ga_{0.7}As$ heterostructure channels, the conductivity of in-plane-gated channels in $In_{0.1}Ga_{0.9}As$ is not improved significantly by the thermal annealing process, which means that the depletion lengths remain essentially constant. We show that the ion beam blanking has a critical influence on the quality of the channels. If the beam blanking creates an ion "tail" across the channel, the effective electron density in the channel is reduced, which decreases both the attainable saturation currents and the transconductance.

We gratefully acknowledge the MBE expertise of Hans-Peter Schönherr and financial support by the Bundesministerium für Forschung und Technologie of the Federal Republic of Germany.

Light Emission in Commercial Pseudomorphic HEMTs

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Submicrometric microwave devices such as MESFETs and HEMTs, when biased at high V_{DS}, experience impact ionization and light emission due to hot electrons [1-3]. By coupling electrical measurements with optical characterization in this work we relate the features of the emitted light spectra with hot electron phenomena occurring in the InGaAs channel of commercial pseudomorphic HEMTs, and present evidence of a band-to-band cold electron recombination peak. Emitted light spectra are measured biasing the HEMTs in the pre-breakdown region with the set-up shown in Fig. 1. The devices under test are Fujitsu pseudomorphic *SuperHEMTs*^{TM}, with channel length $< 0.25\ \mu m$ and 200 μm gate width. The measured $V_{DS} - I_D$ curves at 300 K are shown in Fig. 2; when impact ionization occurs the generated electrons are collected by the drain while holes move towards the gate: therefore I_G gives an estimate of the amount of generated hole-electron pairs [1-3]. The rapid increase of the I_G for $V_{DS} > 3.5\ V$ is thus an indicator of hot electrons giving rise to impact ionization in this bias range. The dependence of I_G on V_{GS} at fixed V_{DS}, illustrated in Fig. 3, shows the bell-shaped behavior commonly observed when impact ionization phenomena take place [2-4]. Fig. 4 reports the light spectra obtained at 300 K and 100 K with $V_{GS} = 0\ V$ and $V_{DS} = 4.4\ V$. The 300 K spectra can be divided in three energy regions (in the 100 K spectrum these regions are shifted to slightly higher energies). *1) Region 1.* At $T = 300\ K$ the low-energy region ($E < 1.3\ eV$) is characterized by a peak at 1.26 eV. At 100 K the peak's position shifts to 1.33 eV. Both the position and the temperature dependence indicate that this peak can be attributed to transitions from the lowest energy state in the conduction band of the $InGaAs$ channel layer (E_1) to the first allowed state of the valence band, i.e. to band-to-band recombination of cold carriers. *2) Region 2.* In the second region ($1.3\ eV < E < 1.4\ eV$) we note, at 300 K, a shoulder placed at about 1.32 eV. A similar feature is reported in [3], where it is attributed to electron transitions from the second quantized state (E_2) in the conduction band: in our 100 K measurement, possibly due to negligible occupation of E_2, the shoulder disappears and a sharper peak is observed. The distance between the 300 K peak and shoulder is approximately 60 meV, a reasonable value for quantized level splitting in a quantum well channel. *3) Region 3.* The high-energy emission ($E > 1.4\ eV$) shows a rather noisy, nearly Maxwellian distribution, which is generally attributed to hot electron recombinations. In order to clarify the emission mechanisms of high-energy photons, integrated light intensity has been measured for $E > 1.5\ eV$ as a function of V_{GS}. Previously published measurements [2] showed a linear dependence of the integrated light intensity on $I_D \times I_G$, i.e. on the product of electron and hole concentrations; this was claimed to prove that recombination of hot electrons was the main cause of light emission. To investigate this point, in Fig. 5 we plot the dependence of the integrated light intensity at 300 K and 100 K on $I_D \times I_G$. A reasonably linear dependence is shown for $-0.3\ V < V_{GS} < 0.1\ V$. A marked deviation from linearity is instead observed outside this range at 300 K. Non-linearities, however, can be expected both at low V_{GS}, when the gate bias approaches the pinch-off voltage, and at high V_{GS}, due to reduction of the electric field that drives the holes towards the gate.

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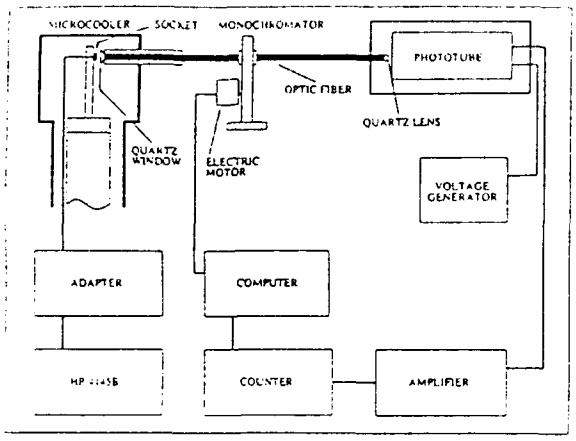

Figure 1: Measurement equipment.

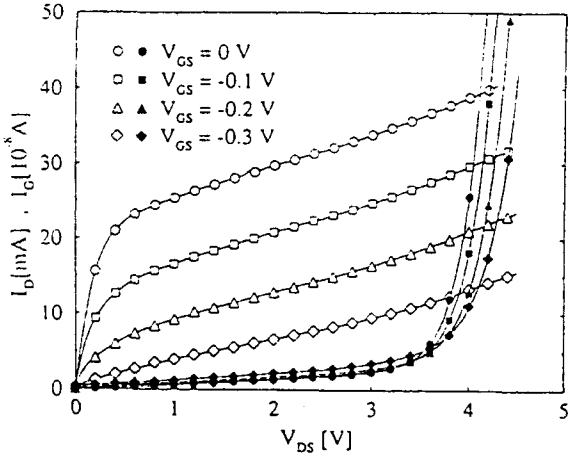

Figure 2: Drain (open symbols) and gate (full symbols) currents of a Fujitsu *SuperHEMT*^{TM} versus V_{DS} for various V_{GS}; $T = 300\ K$.

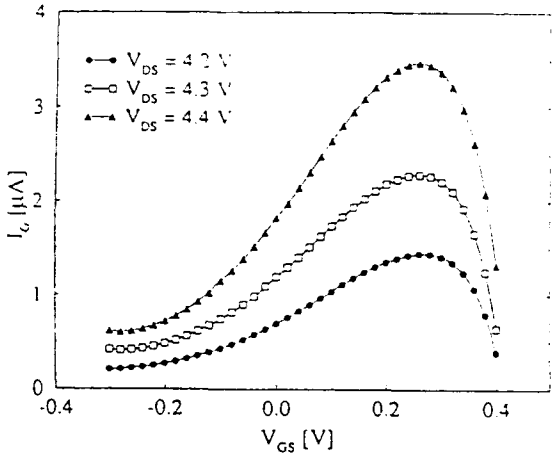

Figure 3: Gate current versus V_{GS} at different values of the drain bias; $T = 300\ K$.

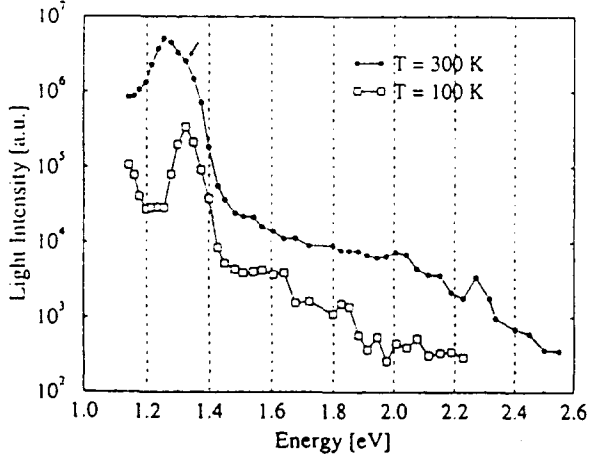

Figure 4: Emitted light spectra at $T = 300\ K$ and $T = 100\ K$; $V_{DS} = 4.4\ V$, $V_{GS} = 0\ V$. The arrow marks the position of the shoulder.

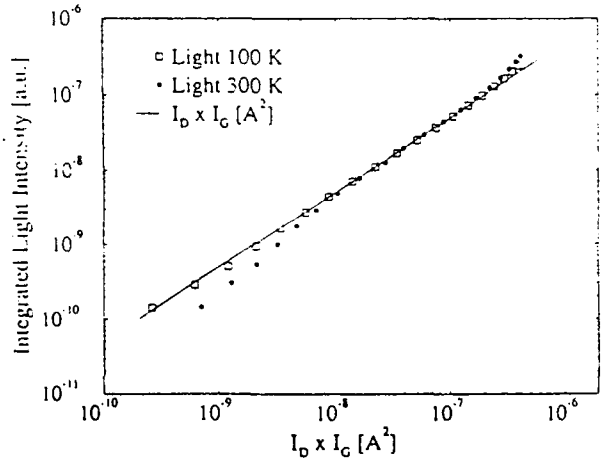

Figure 5: High-energy ($E > 1.5\ eV$) integrated light versus $I_D \times I_G$ at 300 K and 100 K with $V_{DS} = 4.4\ V$. A solid line corresponding to linear dependence is shown for comparison.

Hot electron luminescence in $In_{0.53}Ga_{0.47}As$ channel transistor

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We report measurements of light emission, in the 1.1-2.5 eV energy range, of hot electrons in $In_{0.53}Ga_{0.47}As$ channel of a complementary CHarge INjection Transistors (CHINT). By comparing electrical characteristics and light emission we are able to identify the conduction to conduction-band transitions as the main light emission mechanism. Hot electrons effective temperature up to 2200K has been determined by using the high energy exponential tail of the electroluminescence spectra.

Samples used are complementary n-channel CHINT implemented in lattice matched InGaAs/InAlAs heterostructure material grown by MBE on InP substrate [1-2]. A schematic cross section of the device and the equilibrium energy band diagram are shown in Fig. 1. The channel length is $L_{CH} = 1$ μm and the channel width is $W = 40$ μm.

With the collector voltage $V_{CS} \leq 0$ V the complementary CHINT acts similarly to a depletion field effect transistor, where the collector layer acts as gate. Figure 2 shows the typical drain I_D and collector current I_C characteristics as a function of the drain voltage V_{DS} at different negative collector biases. For high drain bias ($V_{DS} > 3$ V) Real Space Transfer (RST) of holes created by impact ionization occurs in the channel resulting in a negative I_C. This current increases with increasing V_{DS} and results orders of magnitude larger than the reverse current I_{CDO} of the drain-collector junction measured with the source floating, Fig. 2 dashed line. The impact ionization current, as monitored by I_C, decreases if we apply higher negative V_{CS} since the channel current is reduced by the field effect.

Figure 3 shows the room temperature emission spectra with the device biased at $V_{CS} = 0$ V and different V_{DS}. The intensity of the emitted light increases with increasing the drain voltage. At energies larger than 1.5 eV all spectra exhibits a maxwellian distribution whereas the slope decreases with increasing drain voltage.

In Fig. 4 we compare the light intensity P, integrated over the 1.1 eV to 2.5 eV energy range, with I_D, I_C and $I_D \times I_C$, for a fixed $V_{DS} = 4.5$ V and function of V_{CS}. As the collector bias decreases, I_D also decreases due to the field effect. The light intensity is seen in Fig. 4 to follow both I_C and I_D. This indicates that the light emission mechanism is caused by single carrier transition, hot electrons or hot holes, and not by the recombination between conduction and valence band, which would imply the proportionality of P with $I_C \times I_D$. Two arguments lead to believe that electrons are the carriers responsible for the light emission. First, as the ratio between the magnitude of the drain and the collector current shows, the density of hot electrons in the high field region of the channel is more than two order of magnitude greater than the density of holes. Second, RST of holes above the 0.2 eV ΔE_V are likely reduces the presence of hot holes in the channel.

According to this consideration, we are able to identify the transition of hot electrons in the conduction band being responsible for the luminescence spectra. Assuming that the electron energy distribution are reproduced by the photon energy distribution, effective temperatures can be extracted from the maxwellian slope of high energy tails of the light spectra; they are found to lie in the 920 - 2240 K range.

In conclusion, we have studied the light emission of hot electrons in $In_{0.53}Ga_{0.47}As$ channel of a complementary CHINT in condition of impact ionization. Transitions of hot electrons, in the conduction bands, are identified as the mechanism responsible for the light emission. The slope of the tail of the luminescence spectra indicate an effective temperature for the electrons as high as 2200 K.

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2) M. Mastrapasqua, S. Luryi, G. L. Belenky, P. A. Garbinski, A. Y. Cho, and D. L. Sivco, IEEE Trans. Electr. Dev. 40, 1371, (1993).

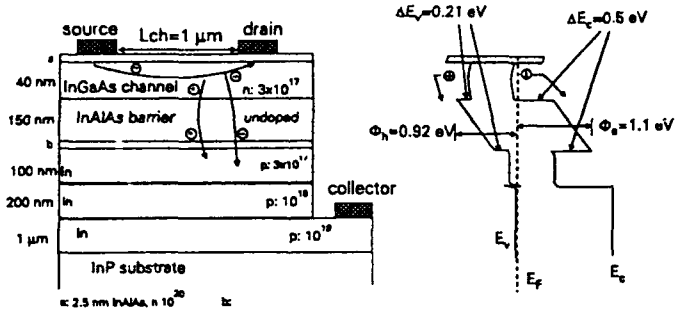

Fig. 1 Cross section of our complementary charge injection transistor structure and its equilibrium energy-band diagram. The downward arrow indicates the RST flux of holes, created by impact ionization, for a bias condition $V_{DS} > 0 \geq V_{CS}$. The doping are in units of cm^{-3}.

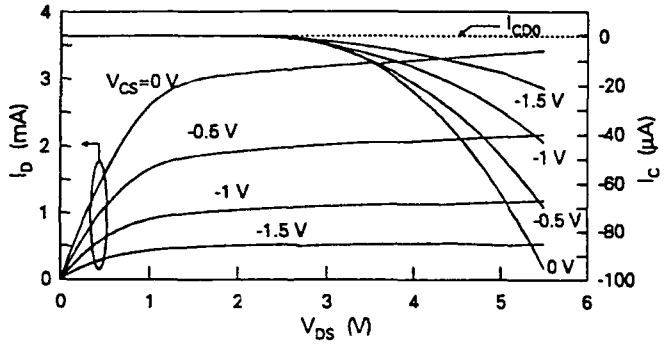

Fig. 2 Room temperature current-voltage characteristics of the devices. The heating bias V_{DS} is varied at different collector biases $V_{CS} \leq 0$ V. The dashed line shows the reverse current I_{CDO} of the collector-drain junction, measured with the source floating.

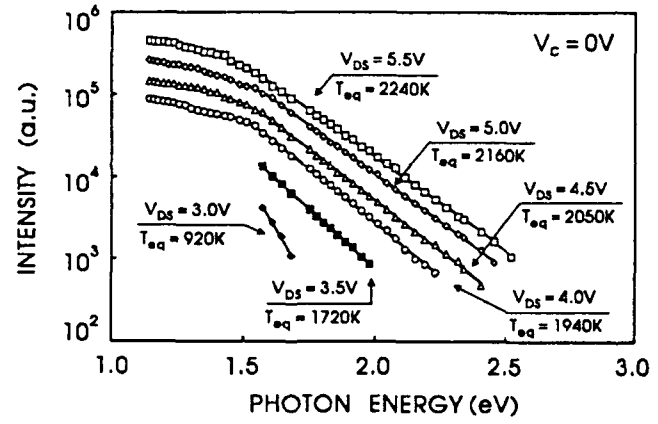

Fig. 3 Spectral distribution of the emitted light as a function of energy at various V_{DS} for $V_{CS} = 0$ V, and lattice temperature $T_L = 300$ K. The effective electron temperatures, T_{eq}, extrapolated from the slope of the spectra (continuous lines) are shown.

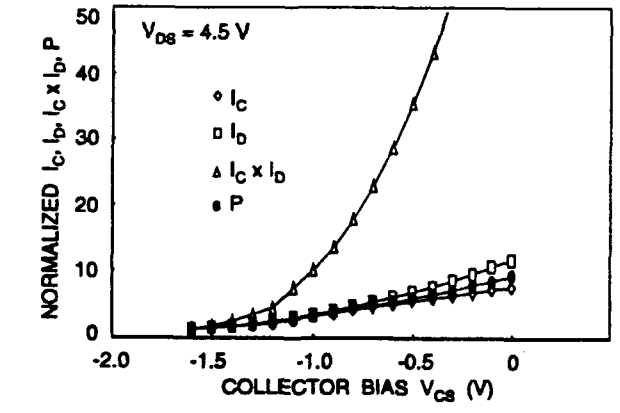

Fig. 4 Collector bias V_{CS} dependence of: light intensity P (integrated over 1.1-2.5 eV energy range), collector current I_C, drain current I_D, and product of the collector by drain current $I_C x I_D$. All the quantities are normalized to their respective values at $V_{CS} = -1.6$ V.

Instabilities induced by DX-centers and impact-ionization hole injection in AlGaAs/InGaAs PM-HEMT's

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AlGaAs/InGaAs pseudomorphic HEMT's (PM-HEMT's) on GaAs are characterized by excellent transconductance, cut-off frequency and noise capabilities up to the millimeter waves [1]. Unfortunately, the small E_g of InGaAs can give rise to increased impact-ionization effects, such as increase in gate current I_g due to generated holes [2], which actually limit power handling capabilities. It is also well known that n-$Al_xGa_{1-x}As$ invariably has electron traps called DX centers [3], which, at low temperatures, can cause collapse of the drain current, kinks in I_d-V_{ds} characteristics, and threshold shifts [4].

Reliability problems related with impact-ionization effects and hot-electron phenomena have been recently observed in AlGaAs/GaAs HEMT's [5]. No data is available on possible degradation effects induced by hot carriers in AlGaAs/InGaAs PM-HEMT. We show that remarkable threshold shift ΔV_P and increase in saturation current ΔI_{ds} can be observed in AlGaAs/InGaAs PM-HEMT's submitted to high temperature (100°C - 200 °C) storage or hot-electron stresses for relatively short times (about 20 hours). Increase in I_{ds} up to 40% have been observed. The increase is not permanent and can be recovered by a room or low temperature storage without bias. We attribute this increase to: (a) thermally-activated detrapping of electrons from the DX-centers; (b) recombination of electrons trapped by DX centers with holes generated by impact-ionization; the consequent reduction in the trapped negative charge induces a shift in the threshold voltage and the observed Ids increase. This room-temperature degradation mechanism of PM-HEMT's is described here for the first time.

The devices characterized in this work are L_g=0.25 μm, W_g=200 μm Mitsubishi MGF4317D PM-HEMT's, adopting a 420 Å $Al_{0.2}Ga_{0.8}As$ donor layer and a 150 Å $In_{0.18}Ga_{0.82}As$ channel [1]. When biased at high Vds, a large increase in (negative) Ig is observed due to collection of holes generated by impact-ionization in the channel, see Fig. 1.

After 22 hours of storage at T=175°C without applied bias, a remarkable increase in I_{ds} is observed, as shown in Fig. 1; this increase is due to a threshold voltage shift and is accompanied by a decrease in I_g and I_{gdo} (not shown). A similar increase in I_{ds} is observed also when the device are submitted to hot-electron accelerated tests; Fig. 2 shows the amount of Ids increase for various tests performed at Vds=4.7 V for 15 hours. The impact-ionization current I_g was changed by varying V_{gs}. ΔI_{ds} increases with I_g, then saturates, and eventually increases again when both thermal effects due to device self-heating and impact-ionization contribute to device degradation. The contribution of impact-ionized holes in accelerating the ΔI_{ds} increase is demonstrated by tests performed at the same dissipated power, but with different I_g; enhanced device degradation was found at high I_g values, Fig. 3 and Table I. An increase in I_{ds} was also observed when holes were generated by gate-drain breakdown, Table I.

For both storage and hot-electron tests the degradation is not permanent, see Fig, 4, indicating a trapping/detrapping mechanism as the possible cause of the degradation. These devices are actually affected by the presence of DX-centers, as demonstrated by noise [1] and pulsed [6] measurements, and by the presence of a kink in the low-temperature characteristics. The negative charge stored on these traps can be removed either by thermal activation of trapped electrons or by recombination with holes generated by impact-ionization [3],[4], thus causing the observed instabilities in I_{ds} and V_P. When the device is stored at room (or lower) temperature, electrons slowly fill the ionized traps and I_{ds} and V_P recover to their original value. In conclusion, we have shown that the presence of traps induces long-term instability effects in AlGaAs/InGaAs PMHEMT's; the described failure mechanism is accelerated by high temperature and impact-ionization effects, and therefore requires particular consideration during the design and application of power devices, which typically operate at high V_{ds}, high dissipated power and T_{ch}.

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Table I: Increase in saturaton current I_{ds} observed during accelerated tests at P_d=98 mW and in gate-drain breakdown conditions with source floating.

Test point in Fig. 3	A	B	C	breakdown
Dissipated power, P_d	98 mW	98 mW	98 mW	0.375 mW
I_g during test	-47.13 μA	-77 nA	+756 nA	-48 μA
ΔI_{ds} during test	+9.4%	+3.18%	0.2%	-
ΔI_{ds} (V_{ds}=1.4V; V_{gs} = 0V)	+10.9%	+4.5%	+3.2%	+6.9%
ΔI_{gd0} (V_{gd}=-5.3V, I_s=0 mA)	-53.6%	-15%	-11%	-62 %

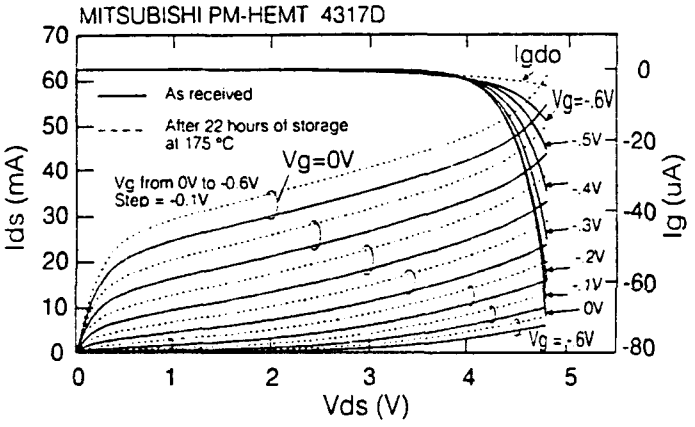

Fig. 1 Continuous lines: I_d and I_g in a "as received" device: I_{gdo} is the gate-drain reverse current, measured with source floating. Dotted lines: I_d after 22 h. of storage at T=175°C.

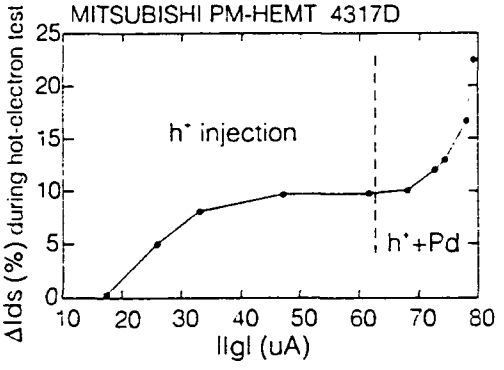

Fig. 2 ΔI_{ds} as a function of impact-ionization hole current $|I_g|$, for tests at V_{ds}=4.7 V, t= 15 h.

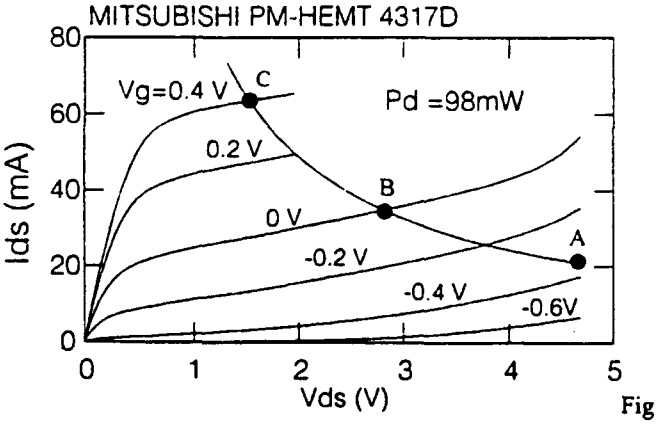

Fig.3 I_d characteristics superimposed to the load line that identifies P_d=98 mW; A,B and C are the various test points.

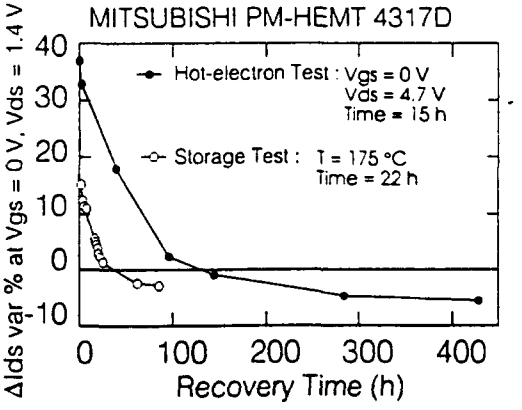

Fig. 4 Typical 300 k I_{ds}-recovery characteristics after storage and hot-electron tests.

Role of Hot Electrons in Subsurface Burnout in GaAs FETs

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Subsurface burnout has been observed in GaAs power FETs, GaAs TEDs, and in some cases when FETs and HEMTs are irradiated with alpha particles. Monte Carlo simulations have shown that hot electrons play an important role in subsurface burnout by making a large contribution to the lattice heating rate. The response of a GaAs FET to an alpha particle passing through the center of the gate has been studied theoretically by means of the Monte Carlo particle model. The angle of incidence from the normal to the epilayer surface has been varied from zero to 60 . Both source and drain were grounded and the gate biased at pinch-off. The gate response currents peak immediately on impact of the a particle and then again as the particles generated by the hit reach the drain or source; the time this takes place depends on the angle of incidence of the particle. By accounting for the exchange of energy between the carriers and the semiconductor crystalline lattice, we find that the actual lattice heating rate culminates near the source and drain on arrival of the induced particles. This may favor filamentary migration of the metallization into the semiconductor material and eventual subsurface burnout by a thermal runaway process.

EVALUATION OF PHEMT REABILTY

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ABSTRACT

In radio link applications it is important to predict, during the design phase, the electrical performance of low noise amplifiers when they are employed in a real system.To this aim, the variation of scattering and noise parameters when these devices are subjected to strict life tests must be determined [1] [2].

An experimental set-up has been arranged that uses Hewlet-Packard instruments and can work from 45 MHz to 26,5 GHz. Its block diagram is shown in fig. 1. This system is computer controlled and the elaboration of measurements is performed with IRE approach [3] [4].

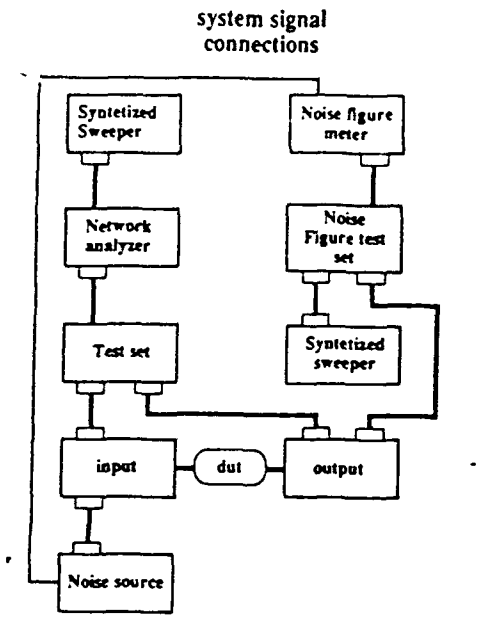

Fig 1 Block diagram of set-up

A detailed description of a Pseudomorfic HEMT (PHEMT) can be found in literature [5], but the most important equations governing his behaviour are reported below:

$$I_{ds} = \begin{cases} I_{dFet} & \text{for } V_{gs} \le V_{pf} \\ I_{dFet} - \dfrac{\xi}{\psi+1}(V_{gs}-V_{pf})^{\psi+1} f(V_{ds}) & \text{for } V_{gs} > V_{pf} \end{cases}$$

$$g_m = \begin{cases} g_{mFet} & \text{for } V_{gs} \le V_{pf} \\ g_{mFet} \cdot f(V_{ds})\xi(V_{gs}-V_{pf})^{\psi} & \text{for } V_{gs} \ge V_{pf} \end{cases} \qquad [5]$$

where ξ and ψ are empirical transconduttance degradation parameter

In this work, microwave noise and scattering parameters over 2 - 26 GHz along with continuous current characteristics have been measured on a PHEMT chip to estimate, in particular, the noise degradation during termal cycles, according to MIL-STD 883 D/B.

Figs. 2 and 3 show, respectively, the variation after 3 thermal cycles and the percent variation of the noise figure vs. frequency for the same device.

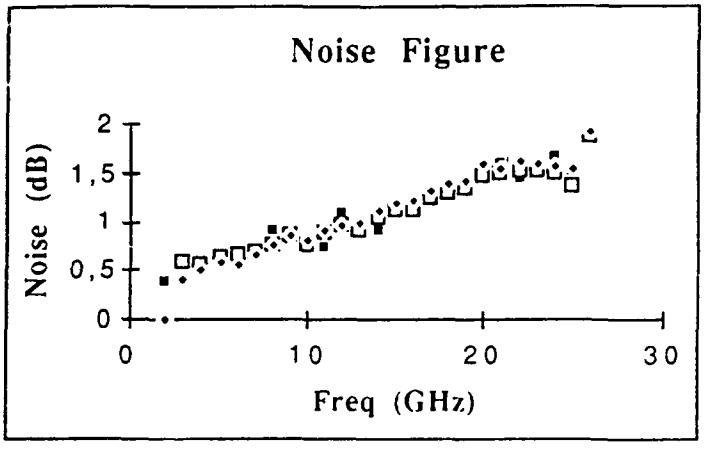

Fig. 2 Variation of Fmin after 3 cycles

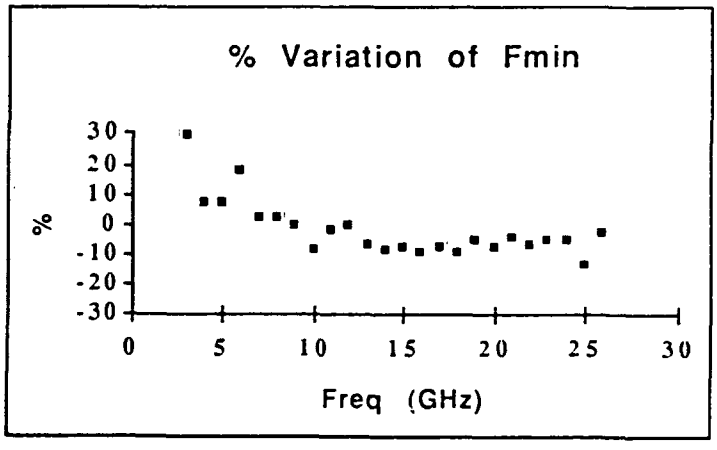

Fig. 3 Variation % of Fmin

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Session 4: OEICs

Chair: H. Thim (University of Linz)

1. **B.Raynor**, Th.Fink, K.Köhler, V.Hurm
   Fraunhofer Institute — Germany
   Integration of 1.3μm InGaAs/GaAs/AlGaAs HEMT electronics for OEIC receiver circuits

2. **M.Schier**, C.Cremer, G.Baumeister, G.Ebbinghaus, J.Rieger
   Siemens — Germany
   DWDM receiver with integrated SOA/grating spectrograph/photodiode array

3. **G.O'Sullivan**, T.Aherne, E.McCabe, J.Hegarty, P.Horan, B.Corbett
   Hitachi, Trinity College Dublin, NMRC — Ireland
   The monolithic integration of quantum well HEMTs and asymmetric Fabry-Perot optical modulators

4. **H.Großkopf**, F.Besca, F.Grotjahn, I.Gyuro, D.Kaiser, J.-H.Reemtsma, W.Kuebart
   Alcatel — Germany
   Realization and performance of three different InP-based receiver OEICs for 10Gb/s

Integration of 1.3-µm InGaAs Photodetectors and AlGaAs/GaAs/AlGaAs HEMT Electronics for OEIC Receiver Circuits

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We will present the process technology for manufacturing 1.3-µm-wavelength optoelectronic receiver circuits consisting of InGaAs MSM photodetectors which are monolithically integrated with HEMT electronics on GaAs substrates. The starting point of device fabrication is the MBE growth of our standard double-pulse doped AlGaAs/GaAs/AlGaAs quantum well HEMT structure on GaAs substrate for enhancement and depletion FETs. On top of this HEMT structure, the photodetector layers are grown which are basically a thick low-temperature (T = 200 °C) InGaAs layer capped by thin GaAs/AlGaAs layers for improved Schottky barrier characteristics of the MSM contacts. Between the InGaAs and the top layer of the HEMT structure, a 3 nm AlGaAs etch stop and 300 nm of undoped GaAs are grown to enable well-defined removal of the detector layers structure for processing of the buried HEMT structure.

In the following, the essential process steps for photodetector-HEMT integration will be outlined. The first step is the definition of interdigitated MSM photodetectors by direct-write electron-beam lithography using a two-layer resist. To avoid proximity effects, the minimum distance between adjacent detector fingers has to be 1.0 µm. After developing the resist, the Schottky metal fingers (Ti/Pt/Au) are fabricated in a conventional lift-off technique.

Before FETs can be processed, the photodetector layers have to be removed on most of the wafer so that mesas of approximately 1 µm height remain around the MSM diodes. This is achieved by using a non-selective wet solution (H_3PO_4:H_2O_2:H_2O) to etch the cap layer, the LT-InGaAs, and part of the underlying buffer layer of undoped GaAs. The remaining part of this layer is then selectively removed by reactive ion etching using CCl_2F_2. The etching comes to an end as soon as the AlGaAs etch stop layer on top of the HEMT structure is reached. After selective removal of this layer by means of an HCl:H_2O_2:H_2O dip, the receiver electronics can be fabricated according to the standard HEMT process developed in our institute.

Transistor gates of 0.2 and 0.3 µm length are defined by means of electron-beam lithography using a two-layer resist; for all other metalization levels, optical contact lithography is applied. Device isolation is achieved by oxygen ion implantion. Finally, for interconnecting photodetectors and electronics, air bridges according to our standard process are used. A schematic picture of an optoelectronic receiver circuit fabricated by the described procedure is shown in Fig. 1.

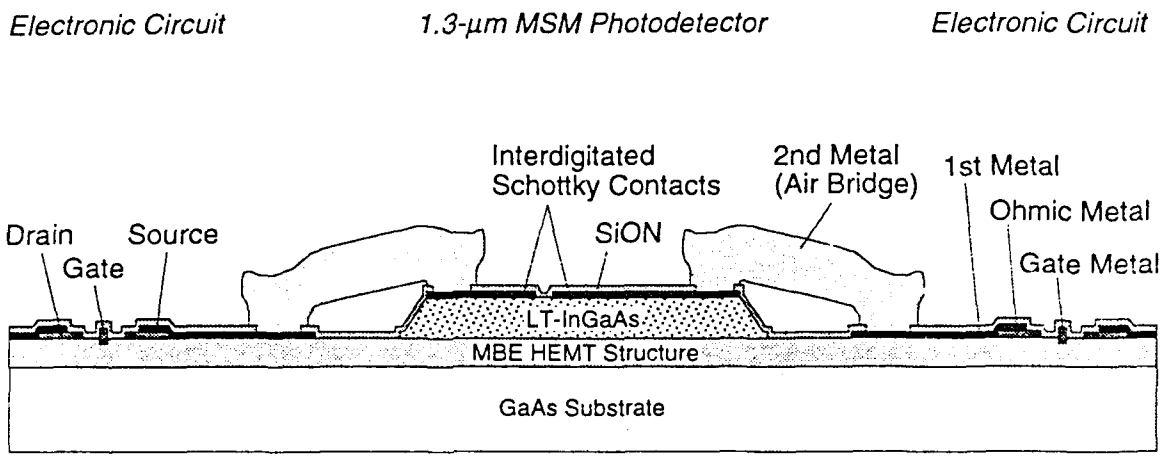

Fig. 1. Schematic picture of 1.3-μm photodetector with HEMT electronics.

DWDM receiver with integrated SOA/grating spectrograph/photodiode array

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Introduction

Wavelength division multiplexing (WDM) offers an excellent application for optical fibres in fibre-optic interconnections, both in optical communication [1] as well as in local area networks [2]. Hereby the very high bandwidth is one of the major advantages of DWDM systems. For simultaneous separation and detection of different wavelength channels grating type demultiplexers monolithically integrated with photodiode arrays are used [3]. To compensate the rather high on-chip attenuation an optical amplifier may be integrated on the chip. We present here our first results on the integration of a semiconductor optical amplifier (SOA) with passive waveguides, a planar grating demultiplexer and a photodiode array in InGaAsP/InGaAs/InP.

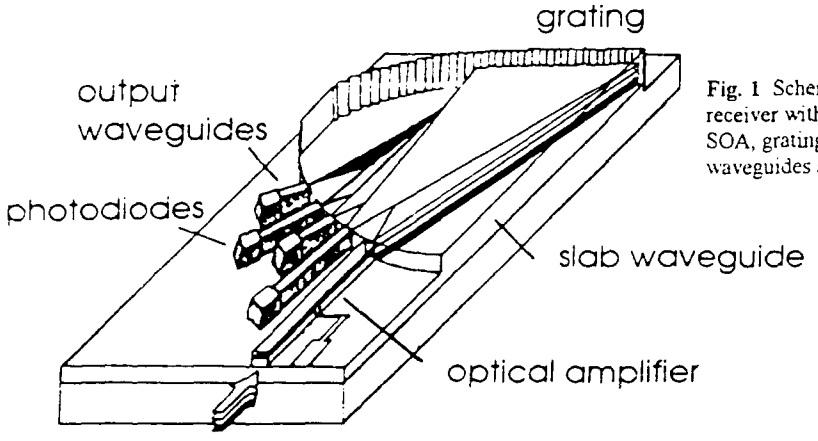

Fig. 1 Schematic view of a DWDM receiver with monolithically integrated SOA, grating demultiplexer, passive waveguides and pin-photodiode array.

Design and Technology

Fig. 1 shows a schematic view of the DWDM receiver with monolithically integrated SOA, grating spectrograph, output waveguides and photodiode array. The light from the fibre is coupled into the cleaved facet of the optical preamplifier. From the other end of the SOA it diverges freely in the slab waveguide. At the blazed and curved grating the light is diffracted and focused into the output waveguides leading to the vertically integrated photodiodes. The complete structure is prepared by a 3 step MOVPE regrowth technology combined with 8 RIE etch-steps.

Semiconductor optical amplifier

On the presented chip a buried heterostructure (BH) semiconductor optical amplifier is used [4]. Between two InGaAsP guiding layers with a gap wavelength of 1.36 µm and a thickness of 0.1 µm the active layer with a gap wavelength of 1.54 µm and a thickness of 0.35 µm is embedded. This basic sandwich structure is grown with some additional etch stop layers on n-doped InP substrate by MOVPE. Using CH_4/H_2 RIE with mass spectroscopic endpoint detection a 1.2 µm wide waveguide stripe is etched. This stripe is overgrown with a p-doped InP layer of approximately 2 µm thickness and a thin p-doped ternary contact layer. To reduce contact resistance these two layers are additionally p-doped by a selective Zn diffusion through a Si_3N_4 mask. Ti/Pt/Au was used as p contact metallisation.

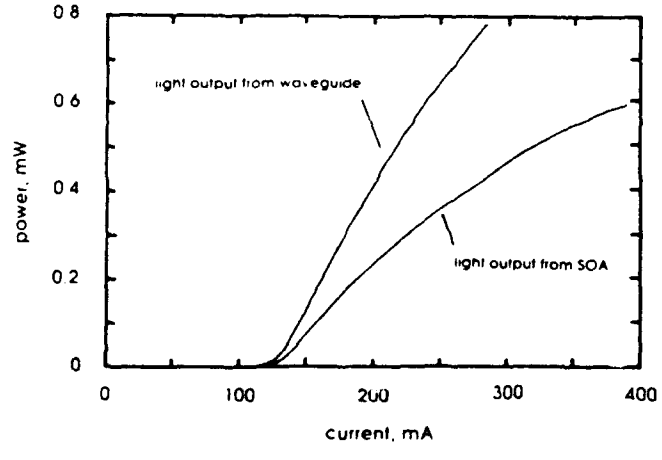

Fig. 2 Light/current characteristics for SOA endface and passive waveguide endface.

Grating

The planar spectrometer consists of a slab waveguide with a curved and blazed grating designed with 2 nm channel spacing for 8 wavelengths (1529 nm, ..., 1543 nm). The slab waveguide is made of a 0.8 µm thick InGaAsP (λ_g = 1.05 µm) layer grown on an undoped InP buffer. To minimize polarisation dependency this quaternary layer is covered by a 1.0 µm thick undoped InP layer. To improve the steepness of the etched grating a $CH_4/H_2/O_2$ RIE process is used [5], which results in sidewall angles of approximately 90°. To achieve high diffraction efficiency the grating is finally metallized with gold.

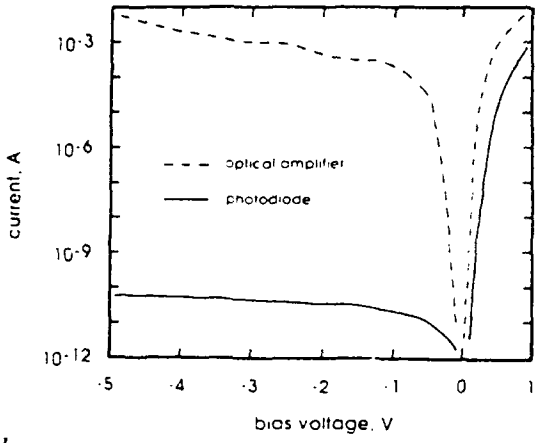

Fig. 3 Dark current of photodiode and optical amplifier.

Photodiode array

The photodiodes are evanescent field coupled through an 0.3 µm thick InP layer to the passive $Q_{1.05}$ waveguide. The 0.63 µm thick InGaAs absorption layer is covered by a 1 µm thick n-doped InP layer and a thin ternary contact layer. CH_4/H_2 RIE with endpoint detection is used to form the photodiode mesas. The pn-junction is obtained by selective Zn diffusion through a Si_3N_4 mask simultaneously with the contact diffusion for the SOA structure. As p contact metallisation Ti/Pt/Au is evaporated and structured by conventional lift off technique.

Results

Fig. 3 shows the light current characteristics of an uncoated SOA/waveguide structure. The light output at the SOA endface and at the passive waveguide endface were measured. The threshold current of the optical amplifier is 120 mA. Due to the lower reflectivity of the SOA/waveguide interface compared to the cleaved SOA/air interface the light output at the passive waveguide endface is higher. It also indicates a quite low attenuation of the light in the buried heterostructure waveguide. In Fig. 3 the dark current of a photodiode compared with the dark current of an optical amplifier as a function of the applied voltage is shown. The best photodiodes exhibit dark currents of less than 100 pA at 5 V reverse bias. Typical values are between 1 nA and 10 nA whereas the SOA shows more than 1 mA at 5 V reverse bias. The measured capacity of the photodiode is less than 0.8 pF. For high bit rate applications a thick intermediate layer (e.g. polyimide) between metallisation and semiconductor surface must be inserted.

Conclusion

First results of a monolithic integration of a semiconductor optical amplifier, passive waveguides, a planar grating spectrograph and a photodiode array will be presented. The uncoated SOA shows a threshold current of 120 mA and a dark current of more than 1 mA at 5 V reverse bias. The vertically integrated photodiodes have a capacity of less than 0.8 pF and show excellent dark currents between 1 nA and 10 nA at 5 V reverse bias.

Acknowledgement

The authors wish to thank J.G. Bauer and G. Kristen for helpful discussions and H. Huber and W. Kunkel for technical assistance. This work has been partly supported by the RACE programme R 2070 MUNDI.

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The Monolithic Integration of Quantum-Well High Electron Mobility Field Effect Transistors, and Asymmetric Fabry-Pérot Optical Modulators

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Abstract

We will discuss a novel high speed smart pixel structure which integrates a high electron mobility transistor with an asymmetric Fabry-Pérot optical modulator. Its use in an optoelectronic amplifer circuit will be also described.

Summary

Monolithic integration of electronic components with optical elements provides a means whereby practical optoelectronic data processing may become a reality. Following recent interest in smart pixels [1,2,3,4] we have developed a novel wafer structure (figure 1) which combines an AlGaAs p-i-n detector/modulator structure and a quantum-well high electron mobility transistor (QW-HEMT) structure.

The complete configuration is that of a modified asymmetric Fabry-Pérot modulator (AFPM) allowing high contrast reflection modulation and efficient photodetection. We grow the QW-HEMT layers inside the AFPM cavity on top of an undoped back mirror. This design avoids the presence of a p-n junction under the QW-HEMT which would otherwise result in backgating [1]. Backgating reduces the output optical contrast ratio and gives rise to a gradual switching action. It arises when a continuous p-layer under more than one n-channel device is held at a fixed voltage. A more complex solution involves the insulation of selected areas of this layer with proton bombardment and contact formation with Be implantation [3].

The QW-HEMT contacts the quantum well region directly. A deep etch uncovers the QW-HEMT surface for processing. This leaves the p-i-n detectors and modulators as mesas. The structure is flexible in that it permits etching of the front surface in order to adjust the optical resonance. Alternatively it would be possible to grow an additional front mirror to increase the contrast ratio of the output modulation. This approach also facilitates the optimisation of the high speed performance of the AFPM [5]. This, married with the high bandwidth offered by the QW-HEMT, holds great potential for high speed smart pixels.

The fully integrated circuit in figure 2 demonstrates the basic utility of this structure. Both the detector and the modulator are formed from the same wafer layers. The QW-HEMT structure is designed to be normally-on (depletion mode). The circuit accepts an optical input beam via a p-i-n diode. In the configuration shown the diode acts as a capacitor being charged by the photocurrent. The upper QW-HEMT is connected as an active load. The charge developed in the diode modulates the gate voltage of the lower QW-HEMT. This allows the gate voltage change to induce a larger output voltage shift which is applied to the underside of the output AFPM thereby controlling its reflectance. The circuit may thus function as an optical amplifier since a low power input may control the modulation of a higher power optical output.

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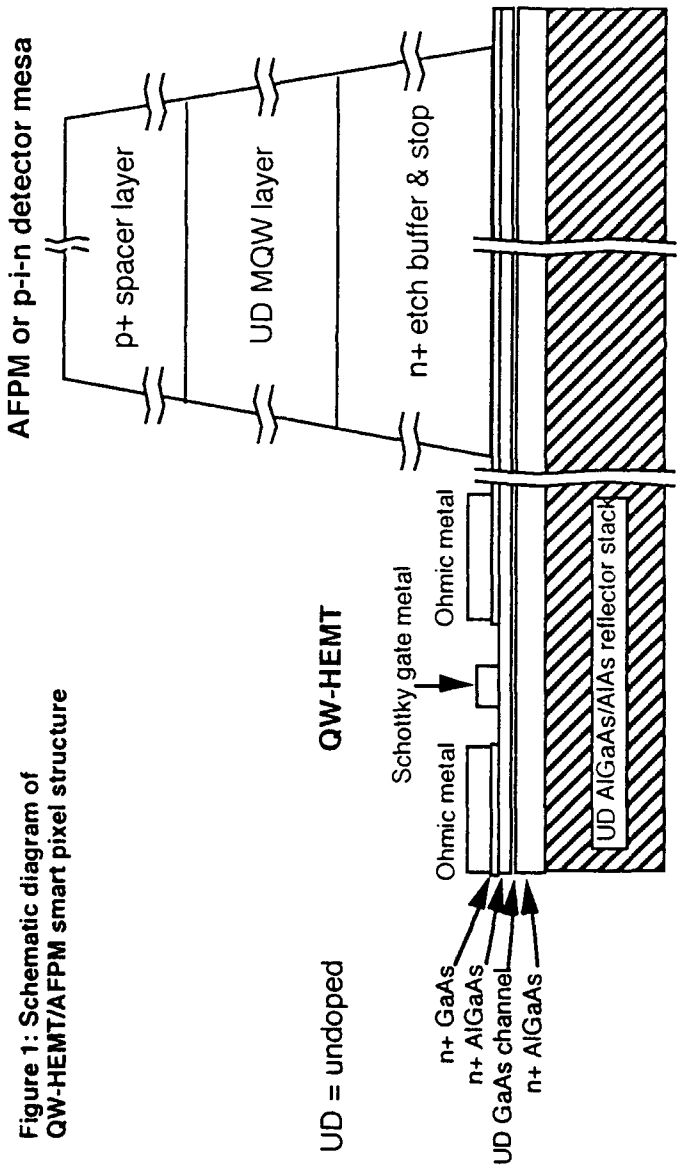

Figure 1: Schematic diagram of QW-HEMT/AFPM smart pixel structure

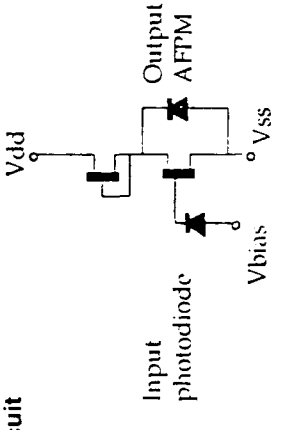

Figure 2: Optical amplifier circuit

Realization and Performance of Three Different InP-based Receiver OEICs for 10 Gb/s

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Monolithic integration of InP based optoelectronic devices for long wavelength fibre communication is of great interest. It is expected to improve reliability, speed and sensitivity at reduced costs for these OEICs, especially for high speed applications.

We have examined three different types of receiver OEICs with increasing circuit complexity, each one designed for 10 Gb/s transmission systems. Prior to realization, circuit simulations for the devices shown in fig. 1 have been performed, based on actually measured device parameters /1/. As a result, the first type, a simple high impedance front end shows the highest noise current (24 pA/√Hz) and there fore the lowest sensitivity (-17.5 dBm for BER = 10^{-9}). The second type, a common gate circuit with its higher sensitivity (-19.2 dBm) is a good compromise between noise performance (15 pA/√Hz) and circuit complexity. The third type,a transimpedance receiver, shows the lowest noise level (9 pA/√Hz) and the highest sensitivity (-21.4 dBm). It has the highest circuit complexity and therefore requires the most elaborate processing.

For the realization of these OEICs we extended our integration process /2/, and incorporated capacitors and level shifter diodes. Process complexity did not increase significantly, since we used already established steps (e.g. the MIM capacitors use the SiO_2 of the AR-coating, the level shifter diodes are realized together with the HEMTs). Using this process we fabricated on the same wafer the above mentioned OEICs as well as several discrete devices for process monitoring.

DC and HF measurements on wafer at these discrete devices are used to determine the characteristics of the elements of the OEICs. Integrated HEMTs with nominal 1* 100 μm^2 gate exhibit an extrinsic transconductance of 300 to 360 mS/mm at a gate leakage current of 2 to 8 µA. Integrated photo diodes have an optical window of 30 µm, they show a bandwidth exceeding 9 GHz (measured at 50 Ω), a dark current around 10 nA and a capacitance of 200 fF at -5V bias.The capacitance of the MIM capacitors is about 7pF with an isolation resistance of better than 500 kΩ.

The high frequency response of the complete OEICs measured on wafer is very flat, even in the case of the transimpedance amplifier (see figure 2). The main results of the measurements are summarized in table 1. Good correspondence between simulated and measured data is found, the difference is generally less than 20%. The spectral noise current density around 3 GHz is very low, 12pA/√Hz being the lowest value reported for an inductance free broadband 10 Gb/s device.

Circuit	$3dB_e$ Bandwidth	Responsivity at 50Ω (0dB=1A/W)	Spectral input noise current at 3 GHz
(HI1) high impedance R_I = 60 Ω	6.1 GHz	2.8 dB	20.4 pA/$\sqrt{Hz}$
(HI2) high impedance R_I = 90 Ω	5.3 GHz	6.5 dB	14.3 pA/$\sqrt{Hz}$
(GO) common gate	6.0 GHz	5.0 dB	15.8 pA/$\sqrt{Hz}$
(TI) transimpedance	5.5 GHz	12.9 dB	12.0 pA/$\sqrt{Hz}$

Table 1: Comparison of four receiver OEICs realized on the same wafer.

In conclusion, we have shown the realization of InP-based receiver OEICs of different circuit complexity. The transimpedance circuit has a high amplification (12.9dB) at low noise (12pA/√Hz at 3 GHz) and a bandwidth of 5.5 GHz.

The work was partially financed by Deutsche Bundespost Telekom.

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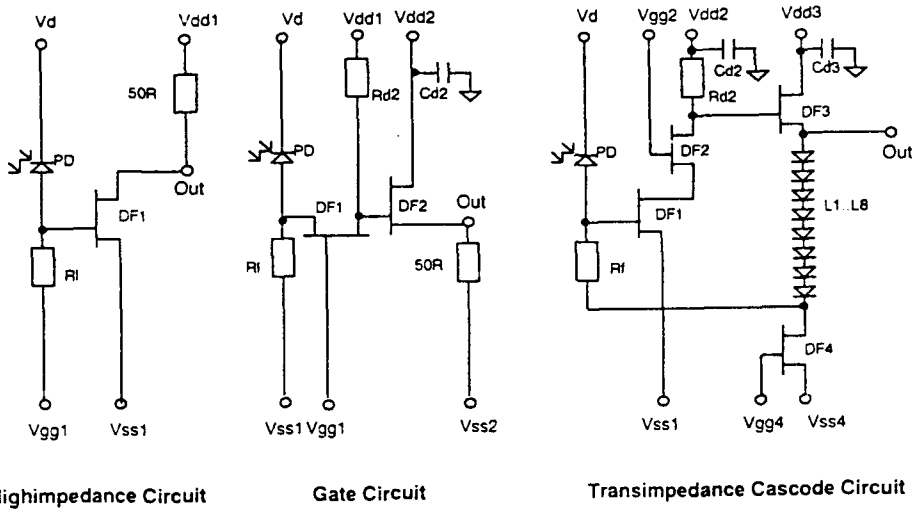

Fig. 1: Circuit diagrams of the examinated three types of OEICs.

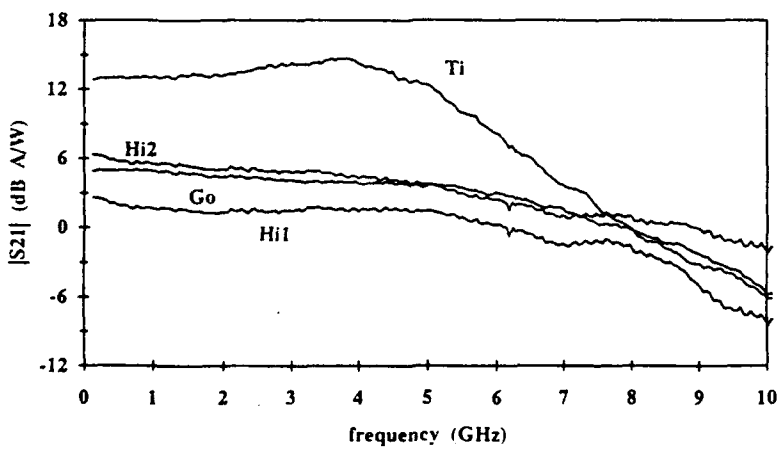

Fig. 2: On wafer measured opto-electronic transfer function (responsivity in dB (A/W)) of four different OEICs (Hi1, Hi2, Go, Til).

Session 5: Transistors 2

Chair: L. Eastman (Cornell University)

1. **Hidetoshi Nishi** (Invited)
   FUJITSU LABORATORIES LTD Japan
   III-V high speed devices

2. **D. Geiger**, J.Dickmann, C.Wölk, E.Kohn
   University of Ulm & Daimler-Benz Research Center Ulm Germany
   Influence of the recess configuration of GaAs-HFET's on feedback and breakdown characteristics

3. W. Prost, U.Auer, F.Scheffer, R.Reuter, C.Heedt, **F.J.Tegude**
   Duisberg University Germany
   InP based HFETs with lattice matched InGaAs channels grown by MBE and MOVPE: Achievements and comparison

4. **H.Heiß**, S.Kraus, Dong Xu, R.Semerad, F.Lautenback, G.Tränkle, G.Weimann, R.Averbeck, H.Riechert
   Walter-Schottky-Institut & Siemens Germany
   InAlAs/InGaAs MODFETs with improved 0.13μm gates

5. **R.J.Trew** (Invited)
   Case Western Reserve University, Cleveland USA
   Gate breakdown and high efficiency power amplifiers for low power applications

6. **J.Braunstein**, P.-J.Tasker, M.Schlectweg
   Fraunhofer Institute Germany
   Equivalent circuit modelling of the cascode connection of MODFETs

7. **C.Bergamaschi**, W.Patrick, M.Schefer, B.-U.H.Klepser, W.Baechtold
   Institute of Technology, Zurich Switzerland
   Fabrication, characterisation and modelling of high performance 0.25μm gatelength InAlAs/InGaAs HEMTs

8. **Paul J.Tasker**, A.Hulsmann, W.Bronner, M.Demmler, J.Schneider, K.Kohler, J.Braunstein, M.Schlectweg
   Fraunhofer Institute Germany
   Pseudomorphic MODFET design optimisation for applications requiring both high power and efficiency

9. **S.Kraus**, H.Heiß, D.Xu, F.Lautenbach, R.Semerad, G.Tränkle, G.Weinmann, R.Averbeck, H.Riechert
   Walter-Schottky Institute, Siemens Germany
   Determination of extrinsic elements in sub μm InGaAs/InAlAs HEMTs

Ⅲ-V High Speed Devices

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ABSTRACT

The role of high speed devices in semiconductor industry is changing very rapidly during these few years with a remarkable change in the system trends of so-called Down-sizing, Networking, and Multi-media going on. Especially, growing demand for mobile communication, WLAN, and PDA requires lower power, lower voltage operation of the high speed devices rather than requiring only higher speed operation as expected before. Since the application of the high speed devices is expected to expand more into consumer products, cost-driving technology development is also becoming more important than used to be.
In this paper, the current development status and possible future role of Ⅲ-V high speed devices, including HEMT and HBT, will be prsented.

HEMT with an InGaP/InGaAs structure will be shown suitable to realize a sub-quater-micron-gate transistor with excellent performance enhancement compared to the conventional AlGaAs/GaAs structure. The K-value of 1250 mA/V^2mm has been obtained at a gate length of 0.15 μm. Sub-ten ps switching will be feasible by this technology. A noise figure of 0.41 dB with an associated gain of 13 dB has been exhibited at 12 GHz for DBS application. A low power dual modulus prescaler has been developed using 0.35 μm, which operates at 2 GHz with 1.2 V single power supply. The device consumes current as small as 1 mA, indicating its usefulness in the battery operating wireless systems.

A self-aligned GaAs based HBT shows very high f_T and f_{max} of 60 GHz and 120 GHz, respectively, although a relaxed design rule of 2 μm is used. Using this technology, both analog and logic ICs marginaly operating at 10 Gbps have been developed for optical fiber communication systems. Also HBT shows more excellent characteristics as a microwave power device than any other competing technologies. Output power of 1 W at 900 MHz with 70 % efficiency can be delivered with a single power supply of 3.5 V, promising important role in the future mobile communication systems.

Complementary HEMT technology as an ultra low power, high speed device will be also discussed.

Influence of the Recess Configuration of GaAs-HFET's on Feed Back and Breakdown Characteristics

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The performance of HFET devices depends strongly on the shape of the recess configuration. A narrow recess towards the source is necessary to obtain a low parasitic source resistance and to allow forward gate bias operation. A wider recess on the drain side of the gate is proposed to reduce C_{GD} and G_{DS}. This leads also to higher V_{GD} breakdown voltages. However, in many cases this is not seen in the maximum open channel source drain voltage. In this contribution an attempt is made to correlate these different phenomena.

Pseudomorphic HFET devices with gatelengths of 0.25µm and an asymmetric recess configuration were fabricated on different layer structures. The recess width towards the drain was varied while the recess width towards the source was kept identical. All devices in this study had similar current ranges and a comparable g_m. The devices were analysed under DC- and RF-conditions from 2 to 40 GHz at various bias points.

The breakdown behavior was measured with 'two terminal' V_{GD} and 'three-terminal' V_{DS} measurements. 'Two terminal' V_{GD} breakdown is defined at 1mA/mm reverse gate drain current, with open source. 'Three terminal' V_{DS} breakdown is defined at 1mA/mm gate current, while the device is biased at $0.5*I_{DSmax}$. A typical output characteristic is shown in fig. 1. The influence of the recess width on the V_{GD}- and V_{DS}-breakdown behavior is shown in fig. 2.

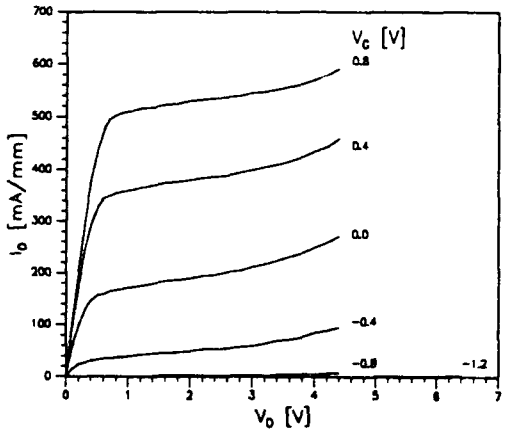

fig. 1: Output characteristic of a device with a 150nm wide recess towards the drain. Note the higher V_{DSmax} at pinch-off.

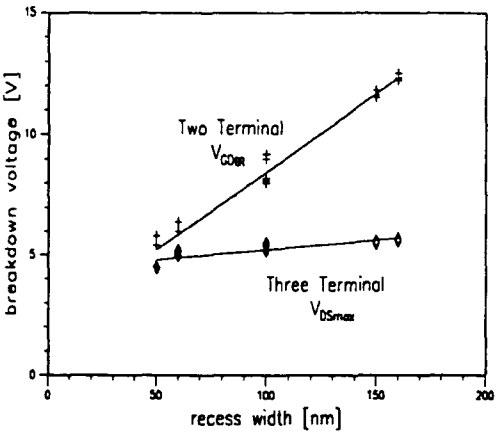

fig. 2: 'two-terminal' V_{GD}- and 'three-terminal' V_{DS}-breakdown of devices with different widths towards the drain.

A wider recess leads to a higher gate drain breakdown voltage, which is however not sustained in active operation while an output current is flowing.

The influence of the recess configuration on the small signal parameters of interest, C_{GD} and G_{DS} is shown in figure 3a and 3b.

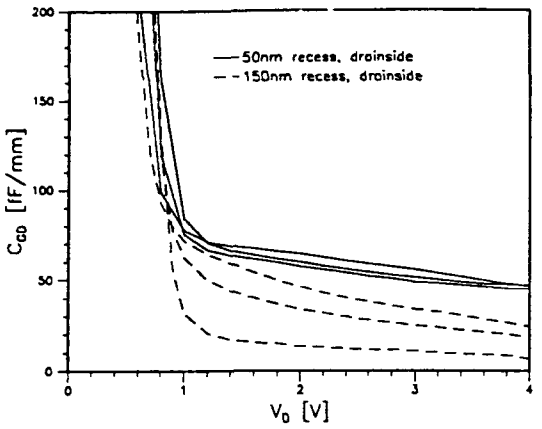

fig. 3a: Development of C_{GD} with drainbias, for different V_G. C_{GD} beyond pinch-off is not plotted, because of the influence of the increased gate leakage.

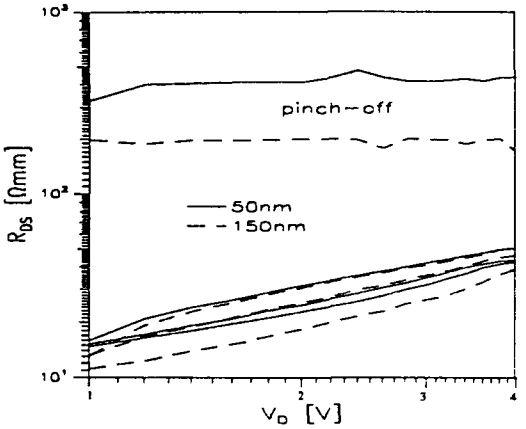

fig. 3b: Development of R_{DS} with drainbias. For different V_G.

Considering $R_{DS}=1/G_{DS}$, it is seen that beyond pinch-off the n-channel/p^--buffer layer junction leads to very low leakage currents. At the open channel condition charge is injected into the buffer layer, bypassing the high field channel region. This high field channel region develops in saturation. Beyond pinch-off it is a lateral space charge layer, at open channel condition it is often refered to as a drift region or a high field domain region. A wider high field channel region will result in a higher bypass resistance [1]. In fact, a linear increase of R_{DS} with drain bias is seen over a wide bias range independent of the recess configuration. Thus, the high field channel region extends freely towards the drain. It seems that the recess configuration does not limit the extension of the lateral space charge layer in either case.

Considering C_{GD} at the same bias conditions a pronounced difference is seen especially at high drain bias, where the capacitance associated with the channel space charge layer becomes small. C_{GD} seems therefore in part determined by a fringing capacitance parallel to the channel space charge layer capacitance and independent of the drain bias. This fringing capacitance may be related to the higly doped or metallic areas of the structure outside of the recess. Thus a wide recess towards the drain is needed to reduce this part. Since the high field drift region and thus the associated capacitance are strongly correlated with G_{DS}, this intrinsic part again is widely independent of the recess configuration.

If the maximum field in the channel space charge layer at the drain edge of the gate determines the maximum V_{DS}-bias, no dependence on the recess configuration is expected. This is indeed seen (fig. 2). Beyond pinch-off however, the field is allowed to stretch out further 2-dimensionaly in the case of a wider recess, and a larger breakdown voltage V_{GDmax} is seen for a wider recess.

To optimize the f_{max} of the device the parasitic gate-drain fringing capacitances need to be reduced by a wide recess towards the drain. To improve the power handling capability however, the extension of the drift region within the recess needs to be optimized.

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InP-based HFETs with Lattice-Matched InGaAs-channels Grown by MBE and MOVPE: Achievements and Comparison

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Abstract

Heterostructure field effect transistors (HFET) on InP-substrates with high on-state breakdown voltage and low output conductance grown by MOVPE as well as MBE have been fabricated. The DC-powers capability of all devices defined by optical contact lithography exceeds 4W/mm. Over a wide range the output conductances are less than 3mS/mm yielding voltage gains of more than 100. The current gain cut-off frequencies of the $0.7\mu m \times 80\mu m$ transistors are higher than 40GHz.

These excellent data were obtained by using the specific advantages of these two epitaxy systems. The different growth modes and layer structures will be compared with respect to the typical problems of the MOVPE and the MBE. Hall data of lattice-matched heterostructures are summarized in tab. 1.

In more detail we will show that a very thin InAlAs-buffer (30nm) and highly strained $Ga_{0.5}In_{0.5}P$ layers are responsible for the power capability of the MOVPE grown HFETs. In the MBE machine high resistive InAlAs-buffers grown at low temperatures improve the on-state breakdown and output resistance. A temperature spike at the buffer/channel interface provided smooth growth fronts prior to channel growth.

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C. Heedt, F. Buchali, W. Prost, J. Fritzsche, H. Nickel, and F. J. Tegude
Extremely low Gate Leakage InAlAs/InGaAs HEMT
Inst. Phys. Conf. Ser. No. 129, Chapter 12, pp. 941-942, 1992

	growth temperature	spacer thickness	Hall mobility at 300K	Hall mobility at 77K
MOVPE	680°C	3nm	12000cm²/Vs	70000cm²/Vs
MBE	520°C	2nm	11800cm²/Vs	52000cm²/Vs

Table 1: Typical Hall mobilities of MOVPE and MBE grown lattice matched HFET layers

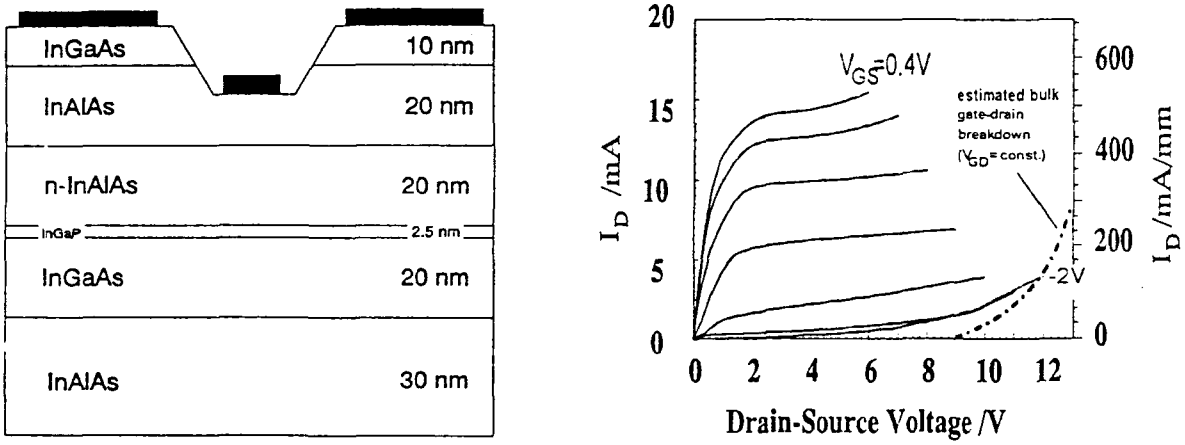

Fig.1: MOVPE grown InP-HFET using an $In_{0.5}Ga_{0.5}P$ spacer
left: layer sequence
right: output characteristics (W_G = 30 µm, L_G = 0.7 µm)

5nm	InGaAs:Si	500°C
20nm	InAlAs	490°C
8nm	InAlAs:Si	510°C
2nm	InAlAs	520°C
20nm	InGaAs	520°C
30nm	InAlAs	540°C
84nm	InAlAs	420°C
	s.i. InP	

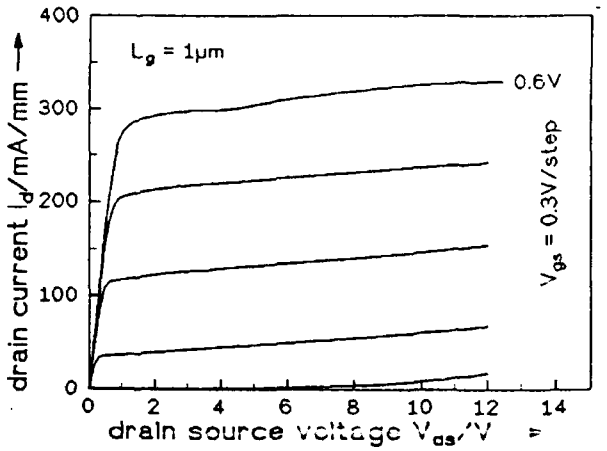

Fig.2: MBE grown InP-HFET using a LT-InAlAs buffer
left: layer sequence
right: output characteristics (W_G = 30 µm, L_G = 1µm)

InAlAs/InGaAs MODFETs with Improved 0.13 µm - Gates

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InAlAs/InGaAs - MODFETs, while showing excellent device performance, often suffer from low and uncontrollable Schottky barrier heights resulting in high gate leakage currents and low breakdown voltages /1/. These gate characteristics can be improved significantly by the incorporation of a thin buried AlAs layer in the undoped InAlAs layer beneath the gate.

Pseudomorphic AlAs layers up to a thickness of 4 nm were used in InAlAs/InGaAs - MODFETs, lattice - matched to InP. All investigated structures consist of undoped InGaAs channels of 32 nm and of 12.5 nm thick InAlAs supply layers, Si - doped to $1 \cdot 10^{19}$ cm^{-3}. Differing undoped layers between the supply layer and the gate were used. The reference sample was grown with 15 nm undoped InAlAs, the other two samples contain AlAs layers of 2 nm and 4 nm, respectively, keeping the total thickness unchanged (see fig. 1). No indication of lattice relaxation was seen. The carrier densities and Hall mobilities of all samples are unchanged, with 300 K values of $3.6 \cdot 10^{12}$ cm^{-2} and 9700 cm^2/Vs.

E - beam lithography with a two -layer PMMA/P(MMA-MAA) resist and selective wet chemical etching with succinic acid, hydrogen peroxide and ammonia were used to fabricate recessed 0.13 µm - T - gates /2/. The selectivity of the etch rates for InGaAs and InAlAs is better than 60 : 1, thus allowing the defined removal of the doped InGaAs cap layer. The self-adjusted gate recess gives an extremely homogeneous gate - channel separation, thus reducing threshold voltage deviations to below 50 mV on the wafer.

Fig. 2 shows the significantly improved Schottky gate behaviour with increasing AlAs thickness. The breakdown voltage determined at I_g = 1mA/mm is increased to - 4.2 V for an AlAs thickness of 4 nm, compared to - 1.3 V in the reference sample. Simultaneously, there is a marked decrease in gate leakage current.

Fig. 3 shows the current - voltage - characteristics of a 0.13 µm - MODFET, with a gatewidth of 150 µm, fabricated from the structure with a 2 nm AlAs layer. No kinks and excellent pinch-off were observed. An extrinsic transconductance of $g_{m,ext}$ = 700 mS/mm was measured. The maximum drain current at U_{ds} = 2 V is I_{DS} = 925 mA/mm. The extrapolation of S-parameter measurements (fig. 4) revealed excellent cut-off frequencies of f_T = 178 GHz and f_{max} = 220 GHz. Further results with δ-doped layer structures will be presented.

[1] S. Wilks, L. Jenkins, J. Morris, S. Clark and R. H. Williams, "Schottky Contacts to InP, InGaAs and InAlAs", 3rd Int. Conf. InP Rel. Mat., Cardiff 1991

[2] Tom P. E. Broekaert and C. G. Fonstad, "AlAs Etch-Stop Layers for InGaAlAs/InP Heterostructure Devices and Circuits", IEEE Transactions on Electron Devices, Vol. 39, No. 3, 3/92.

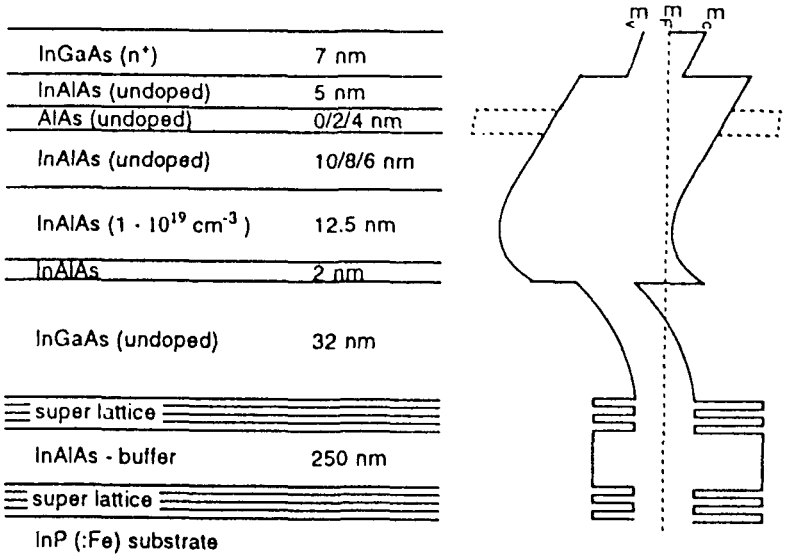

Fig. 1: MODFET layer structure with schematic energy band diagram.

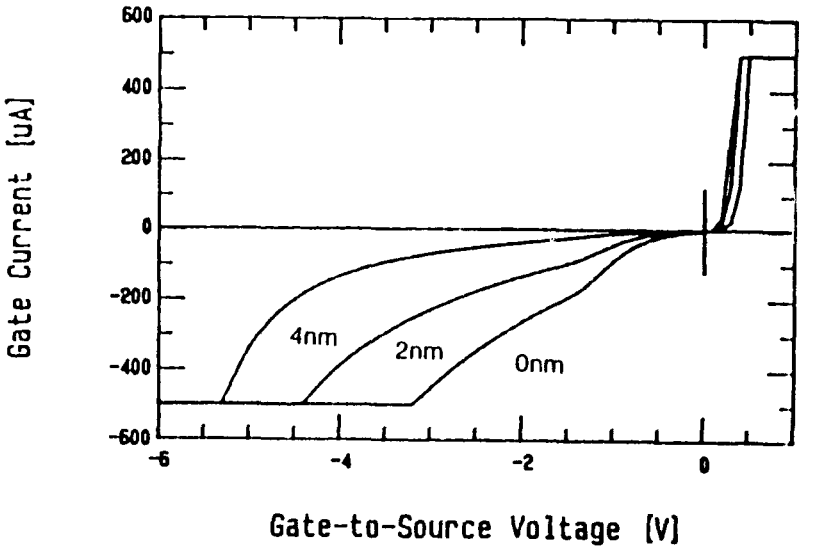

Fig. 2: Diode characteristics improved by 2 nm and 4 nm thin burried AlAs layers.

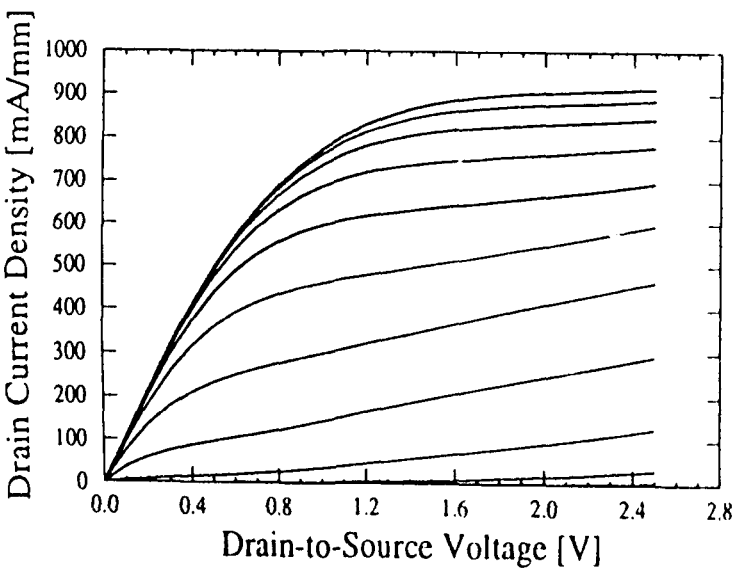

Fig. 3: Drain current density vs drain-to-source bias voltage for a 0.13 x 150 μm^2 (L_G x W_G) MODFET.

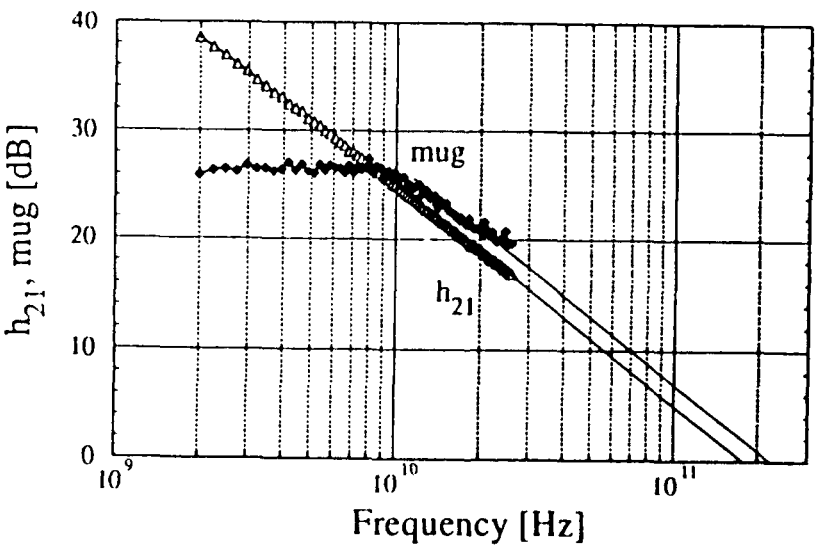

Fig. 4: Extrapolated cut-off frequencies f_T = 178 GHz and f_{max} = 220 GHz. The gate-length is L_G = 130 nm.

Gate Breakdown and High Efficiency Power Amplifiers for Low Power Applications

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Abstract

Mobile systems are rapidly emerging as the dominant communications medium of the future. Cellular telephones, for example, currently have an installed base of over 15 million users and it is predicted that 60% of all communications will be wireless by the year 2000. The emphasis upon portable systems places severe demands upon battery technology and limitations in this area result in demand for low power consumption circuits. Portable transmitters with reduced dc consumption require that very high power-added efficiency devices and circuits be developed. MESFET's are useful for this application. In this work the operation of high efficiency MESFET's is discussed. Forward and reverse gate conduction are shown to be the dominant saturation mechanisms in these devices and a new model for reverse breakdown of the gate electrode is presented. The new model is based upon a tunnel initiated avalanche breakdown mechanism at the gate edge on the drain side. Electrons tunnel from the gate metal into the semiconductor surface area adjacent to the gate. This tunnel leakage current, under the appropriate field conditions, can initiate avalanche breakdown in the surface region. This mechanism generally occurs before bulk breakdown, thereby providing the main limitation to RF voltage that can be sustained. The new model is verified by comparison with experimental data. Incorporation of the new breakdown model into a physics based microwave simulator allows both device and circuit designs that produce optimized power-added efficiency to be determined.

Equivalent Circuit Modeling of the Cascode Connection of MODFETs

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Abstract

The advent of very compact cascodes with short gate length transistors requires a detailed investigation how to model properly this connection of transistors. A simpler approach for longer gate lengths had been presented earlier [1], but it is not sufficient for state-of-the-art MMIC design up to millimeter-wave frequencies. We report about an equivalent circuit model which was derived and validated up to 80 GHz by S-parameter measurements.

Introduction

A cascode is the series connection of two transistors where the input transistor is operated in common source configuration and the output transistor in common gate configuration. The gate of the second transistor is capacitively grounded and can be used for gain control. In this configuration the effective feedback capacitance is minimized by reduction of the Miller feedback effect. Therefore the cascode is an ideal gain element for amplifier design [2].

Cascode equivalent circuit modeling

To allow for a physical relevant equivalent circuit model the physical layout of a cascode must be considered. Obviously the cascode should be modeled as two transistors in one housing. The crucial point is how to describe the interconnections accurately. A SEM-photograph of a cascode in an MMIC is given in Fig. 1. It shows the by only 4 µm separated 0.16 µm long gates of the two stages. The 2.9 µm long connection between them with ohmic metal has a resistance less than 1 mΩ·mm and also a negligible inductance. The contact and semiconductor resistance are comparable to r_s and r_d of MODFETs. For the capacitive grounding of the second gate a series inductance on the order of the gate inductance is taken into account for the model. Other parasitic elements are identical like in the conventional MODFET case.

The derived equivalent circuit model is given in Fig. 2. Fig. 3 shows the good agreement between measured and modeled S-parameters (S_{21} and S_{12}) for frequencies between 1 and 76 GHz.

Comparison between single stage common source and cascoded transistors

As the cascode is the connection of two gain elements with reasonable broadband interstage matching it does deliver more gain than a single common source stage. The superior performance of the cascode with more than 5 dB difference in MSG/MAG is shown in fig. 4. The used wafer area by the cascode is no more than for a conventional MODFET because it is given by the housing (see fig. 1) which delivers the connection to other circuit elements.

Conclusion

An accurate equivalent circuit model for the cascode as a high gain element consuming no more wafer area than a common source stage was established. Successful MMIC designs were realized using cascodes.

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1. J. Wenger, P. Narozny, K. Hruschka, J. Braunstein, and H. Dämbkes, "Low-noise dual-gate cascode AlGaAs/GaAs-HEMTs," 19th International Symposium on GaAs and Related Compounds, 1992, Karuizawa, Japan, Inst. Phys. Conf. Ser., p. 735.
2. J. Braunstein, M. Schlechtweg, P. J. Tasker, W. Reinert, A. Hülsmann, K. Köhler, W. Bronner, R. Bosch, and W. Haydl, "High Performance Narrow and Wide Bandwidth Amplifiers in CPW-Technology up to W-Band," 15th Annual IEEE GaAs IC Symposium, 1993, San Jose, CA., p. 277.

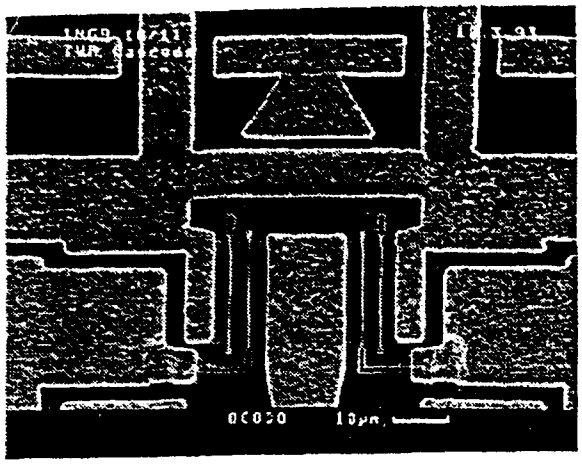


Fig. 1 A cascode pair of transistors in an MMIC.

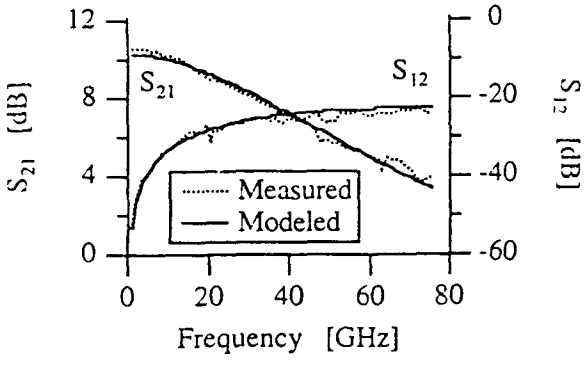


Fig. 3 Measured and modeled S_{21} and S_{12} of a 50·0.16 μm^2 cascode pair of transistors.

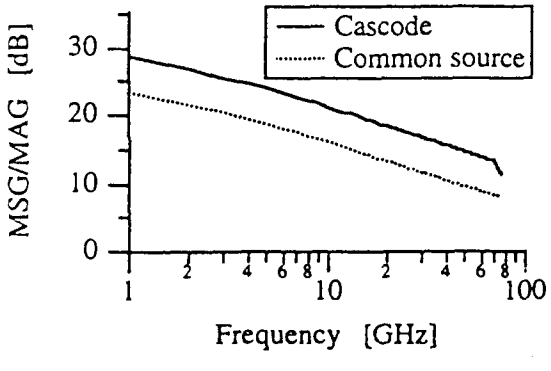
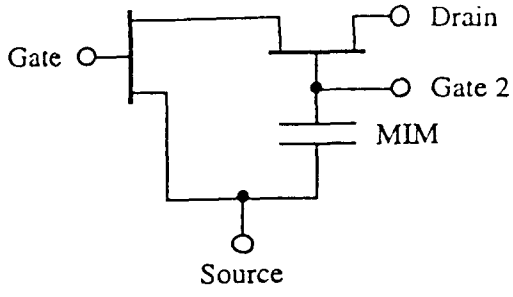


Fig. 4 MSG/MAG for a 50·0.16 μm^2 cascode pair of transistors and a single common source transistor.



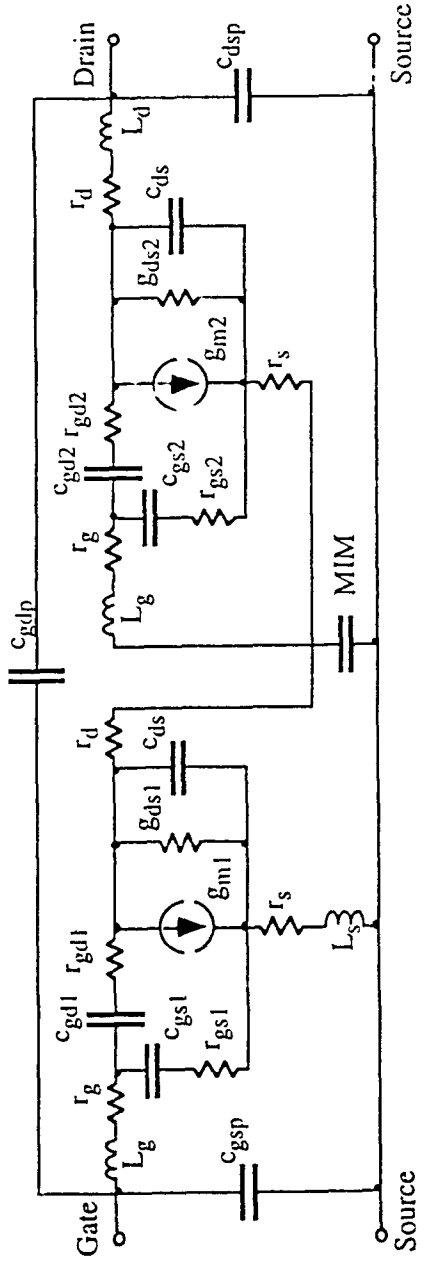


Fig. 2 Equivalent circuit model for a cascode pair of transistors.

Fabrication, Characterisation and Modelling of High Performance 0.25 μm Gatelength InAlAs/InGaAs HEMTs

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Abstract

A reliable process for fabricating MMIC, using 0.25 μm gate-length InP-based HEMT devices, has been developed. The vertical structure of the HEMT was determined with the help of self-developed modelling programme. Crystal growth is carried out by a commercial supplier, using Molecular Beam Epitaxy (MBE). All the processes for latteral pattern definition are carried out in-house using a combination of optical lithography and electron-beam lithography on a modified SEM. Reliable techniques for fabricating ohmic contacts [1] and T-gates have been established, both of which are important for high speed devices. An average transit frequency of 150 GHz has been achieved for quarter micrometer devices which is, to the authors knowledge, a record value for this gate-length (Fig. 1).
Based on a physical device model, a small signal and noise equivalent circuit was developed (Fig. 3). The circuit elements were determined using rf measurements. The noise source parameters were determined using the measured channel noise temperature dependence on the electric field [2] and compared with extracted noise source parameters from noise measurements. A good agreement between measured and modelled parameters was obtained (Fig. 4).
In order to simulate circuits which exploit the non-linear behaviour of these transistors, e.g. mixers and frequency multipliers, a large signal model has been investigated. Fig. 5 shows modelled and measured g_m and R_{ds} as a function of U_{gs}.
The process outline as well as the small and large signal modelling and the noise model will be presented

[1] C.Bergamaschi, W.Patrick, H.P.Meier:"Ohmic Contacts on an InAlAs/InGaAs HEMT-Heterostructure", 16th Workshop on Compound Semiconductor Devices and Integrated Circuits, San Rafael, Spain 1992

[3] C.Bergamaschi, W.Patrick, W.Baechtold:" Noise Temperature as a Function of the Electric Field in an InGaAs/InAlAs HEMT Channel", 17th European Workshop on Compound Semiconductor Devices and Intergrated Circuits, Parma, 1993

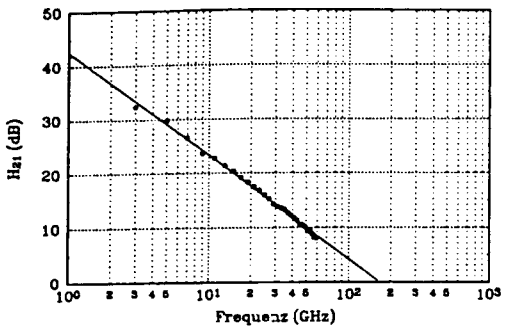

Fig. 1 Current gain versus frequency for a 0.25 µm InAlAs/InGaAs HEMT (U_{ds} = 1.2 V, U_{gs} = - 0.25 V, I_d = 45 mA, Z = 160 µm)

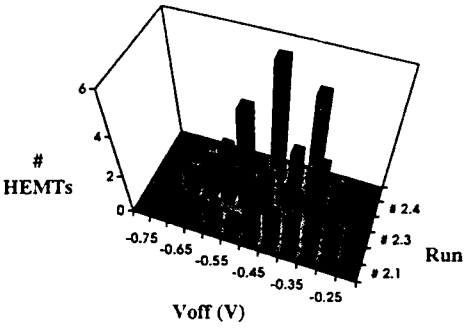

Fig. 2 Threshold voltage distribution of 3 HEMT process runs

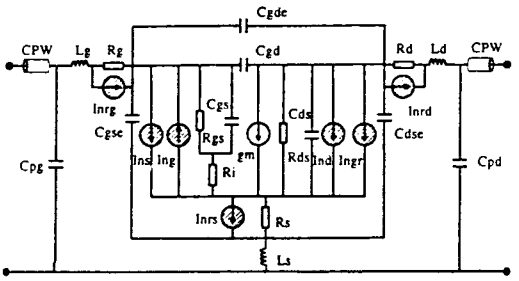

Fig .3 Small-signal and noise equivalent circuit

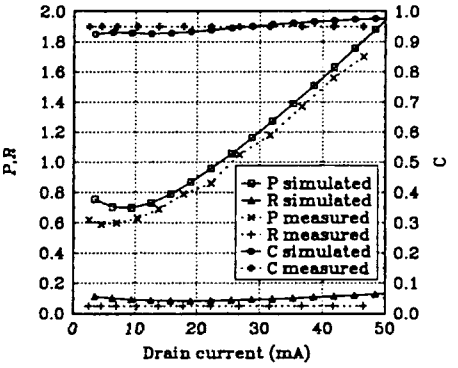

Fig. 4 Measured and modelled noise source parameters as a function of the drain current (Voff = - 0.5 V, L_g = 0.25 µm, d = 25 nm, Z = 160 µm, U_{ds} = 1V, $v_{sat} = 2.6*10^7$ cm^2/s, γ = 1.25, δ = 2.7, D_H = 25 cm^2/s)

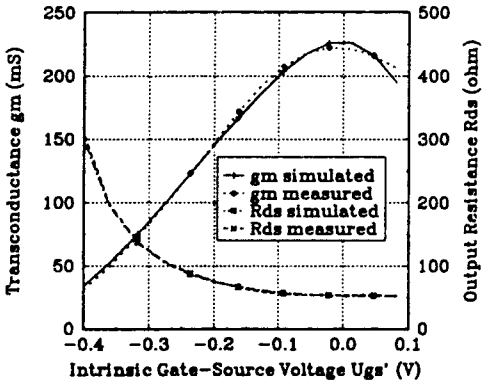

Fig. 5 Transconductance and output resistance vs. gate-source voltage modelled and measured (Uds = 1V, L_g = 0.25 µm, Z = 160 µm,)

Pseudomorphic MODFET Design Optimization for Applications Requiring both High Power and Efficiency

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Abstract: *A novel epitaxial design has been developed to correctly utilize the double doped pseudomorphic MODFET channel in microwave and millimeter wave power transistors. The epitaxial designs investigated, combine the advantageous features of the double doped MODFET channel and a surface depleted cap structure. Short gate length transistors (< 0.3 μm) based on these epitaxial structures provide for both the high current drive > 650 mA/mm and the high source -drain breakdown voltage > 12 V necessary for high power, along with the high gain (> 12 dB) necessary for high efficiency. A high saturated power density, greater than 700 mW/mm, along with a high power added efficiency approaching 50%, were measured between 2 and 20 GHz.*

Introduction: Presently there is considerable demand for transistor structures that can provide both high rf output power (P_{out}) and high power added efficiency (PAE), i.e., mobile communications and phased array radar systems. Short gate length (< 0.3 μm) pseudomorphic MODFET structures should be ideally suited for these applications since they can deliver the high gain (> 9 dB) essential for high power added efficiency. Even though very high current densities are possible in such structures, typically the power densities achieved by these structures are less than desired. Low gate-drain breakdown voltage (< 8 volts) is the major factor limiting their performance.

Transistor Specifications: A theoretical investigation of the transistor specifications necessary to deliver a power density of 750 mW/mm and a power added efficiency greater than 50% indicated that current densities greater than *650 mA/mm are not necessary* but that a drain-source breakdown voltage between 10 - 12 V is essential. An important design constraint, however, is that *breakdown voltage improvement must not be achieved at the expense of gain.* This fact, which is particularly important at millimeter waves, is often forgotten in power transistor design.

Design Concept: Typically in the design of double doped pseudomorphic MODFET structures for power applications the double doped channel is used to increase the maximum current drive of the transistor structure. As shown in figure 1, maximum current densities approaching 1A/mm are possible. However, the theoretical analysis showed that increasing the transistor current drive above 650 mA/mm, the current density possible from a single doped pseudomorphic MODFET structure (see figure 2), is not the key issue. As a consequence, a new design concept has been developed for improved utilization of the double doped MODFET concept for power applications. Channel breakdown in MODFET structures is initiated by tunnel breakdown between the gate Schottky Metal Contact and the highly conducting GaAs Cap layer, resulting in a low gate-drain breakdown voltage (< 8 V), as shown in figure 2. The use of a thin cap layer that is fully surface depleted can eliminate this problem and increase the breakdown voltage (> 15 volts). However, the absence of the highly conducting cap layer in the gate recessed structure also results in very high access resistances. A high access resistance reduces gain and maximum transistor current drive, hence output power and efficiency, which is not acceptable. To obtain a maximum current drive of 650 mA/mm from a recessed gate transistor structure it has been found that the ungated regions must have a current drive greater than 900 mA/mm. The double doped pseudomorphic MODFET channel can be used, in place of the single doped pseudomorphic MODFET channel, to provide this additional current drive in the ungated regions of the transistor. Epitaxial layer designs that combine the double doped pseudomorphic MODFET channel and a surface depleted cap structure in this manner should be optimum for high power and high efficiency applications; providing for high current, high breakdown voltage and high gain.

Experimental Results: Power transistors have been fabricated with such epitaxial structures. They have demonstrated a maximum current drive between 600 and 650 mA/mm with a drain-source breakdown voltage between 10 and 12 V (see figure 3). At 2, 10 and 20 GHz a saturated output

power density of 900, 750 and 700 mW/mm with a Power Added Efficiency (PAE) of 52, 46 and 41 % respectively have been measured on a 200 μm wide transistor into a 50 Ω load (see figure 4). This unfortunately is not the optimum width (W_{opt} = 300 μm) for a 50 Ω load and corresponds to only a rf voltage swing of 7 V. Analysis of the measured data indicates that an rf voltage swing of 10 V is possible, hence a saturated power density of over 1W/mm should be delivered into the optimum load (R_{opt} = 15 Ω-mm) with a power added efficiency around 50% .

Conclusion: An epitaxial layer design concept has been realized that combines a double doped pseudomorphic MODFET channel with a surface depleted cap structure in order to increase the transistor breakdown voltage. In this case, however, a high breakdown voltage is not achieved at the expense of gain or current drive and so it is the optimum epitaxial layer concept for high gain and high efficiency requirements, for both microwave and millimeter-wave applications.

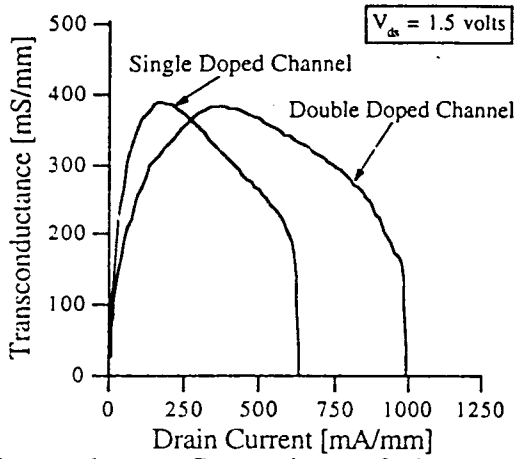

Figure 1. Comparison of the current drive of the single and double doped pseudomorphic MODFET structures (Channel: 120 Å 25% InGaAs, Gate Length: 0.6 μm).

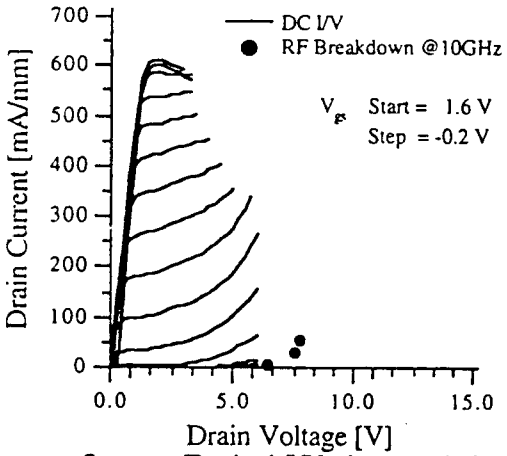

Figure 2. Typical I/V characteristic of a single doped pseudomorphic structure (Channel: 120 Å 25% InGaAs, Gate Length: 0.3μm). While a high current drive is possible a low breakdown voltage (< 7 V) is obtained.

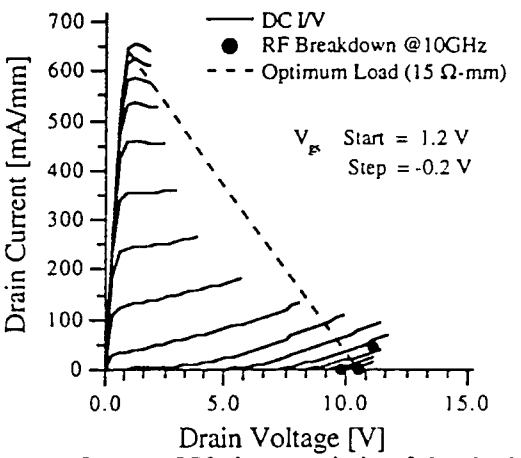

Figure 3. I/V characteristic of the double doped pseudomorphic structure (Channel: 120 Å 25% InGaAs, Gate Length: < 0.3μm) with a surface depleted cap design. A high current drive (> 600 mA/mm) and high breakdown voltage (> 11 V) is obtained.

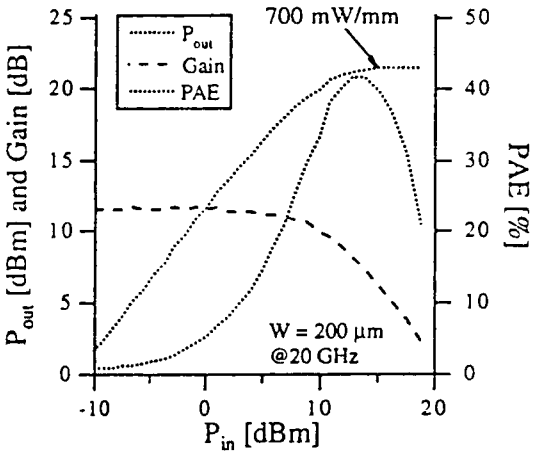

Figure 4. Power performance of the optimized double doped pseudomorphic MODFET structure (Channel: 120 Å 25% InGaAs, Gate Length: < 0.3μm) at 20 GHz. The transistor width is 200 μm and the rf load is 50 Ω, which is not the optimum match for the DUT.

Determination of extrinsic elements in sub-μm InGaAs/InAlAs HEMTs

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For the optimization of sub-μm InGaAs/InAlAs-HEMTs the precise knowledge of the extrinsic small-signal equivalent circuit elements is essential, as they strongly influence the device properties.

Two different approaches for the determination of the extrinsic transistor elements have been used and compared.

The first was the "cold-modeling" /1/ of active high-performance 0.13 μm InGaAs/ InAlAs HEMTs (f_T ~ 200 GHz) with different gate widths (60 μm < W_G < 150 μm), showing cut-off frequencies of 200 GHz. These devices have been fabricated using a reproducible self-adjusted gate recess /2/ and reveal a standard deviation in threshold voltage of ΔU_{th} < 50 mV. From S-parameter measurements at drain-source voltage U_{ds} = 0 and at foreward gate bias resistances and inductances are extracted, at reverse gate bias below pinch off parasitic capacitances are calculated.

The second approach was the high frequency characterization of passive test structures fabricated on semiinsulating GaAs substrates; keeping the contact and gate metallization exactly the same as in HEMTs /3/. Especially the pad capacitances can be determined exactly by comparing test structures with and without gate fingers. As an example the extracted pad capacitances C_{pds} and C_{pgd} are shown in the figure for transistors with different gate width. As expected the pad capacitances are independent of the gate width. For comparison the values extracted from cold-modeling are also shown in the figure; both determination schemes agree very well within experimental errors.

Extracted results for other extrinsic transistor elements will be presented and discussed with respect to the device performance and to the de-embedding of the intrinsic transitor elements.

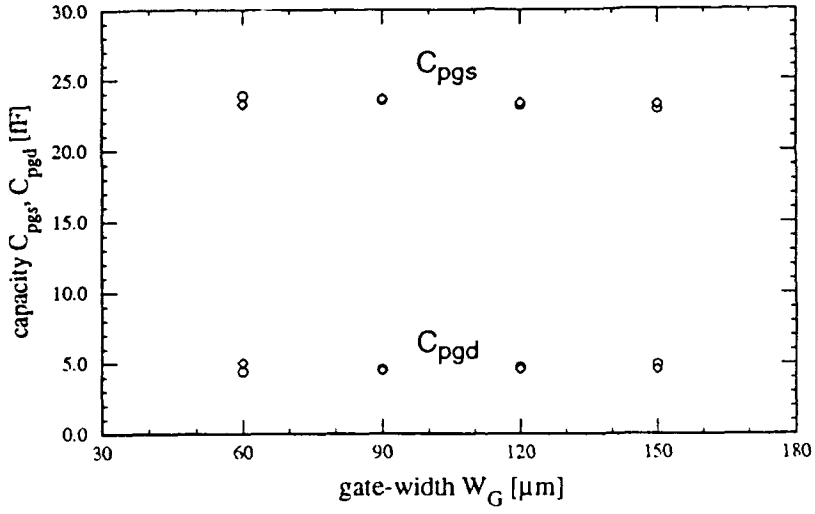

Fig. : Pad-gate-source and pad-gate-drain capacity C_{pgs}, C_{pgd} versus gate width.
circles : "cold-modeling"
diamonds : measurements on semiinsulating GaAs substrates

References :

/1/ R. Anholt and S. Swirrhun: IEEE Trans. on MTT, p.1243f 1991

/2/ H. Heiß, "InAls/InGaAs MODFETs with Improved 0.13 mm - Gates", this workshop

/3/ M. Schlechtweg et. al.: IEEE Trans. on MTT, p. 2445f 1992

Session 6: Two terminal Devices:

Chair: W.M. Kelly (NMRC)

1. A.L.Springer, C.G.Discus, K.Lübke, H.W.Lettenmayer, **H.W.Thim**
   University of Linz — Austria
   Monolithic integrated V-band TED Oscillator

2. **J.Freyer**, T.Bauer
   Technical University of Munich — Germany
   mm wave GaAs impatt diodes using new encapsulation technique

3. **A.Simon**, A.Grüb, V.Krozer, H.L.Hartnagel
   Darmstadt — Germany
   Design and fabrication of a planar THz Schottky diode with quasi vertical structure

4. **D.Pavlidis**, P.Marsh, K.Hong, G.I.Ng
   University of Michigan — USA
   THz Planar Varactor diodes based on InAlAs/InGaAs herterostructures

5. **W.Ebert**, A.Vescan, T.H.Borst, E.Kohn
   University of Ulm — Germany
   Epitaxial Diamond Schottky diode on p+ substrate

6. **A.Matulionis**, V.Bareikis, J.Liberis, I.Matulioniene, A.Oginskas, P.Sakalas, R.Saltis
   Vilnius — *Lithuania*
   Hot electron noise temperature in an n-type GaAs channel at fields over 100kV/cm

7. **D.V.Morgan**, Y.H.Aliyu, A.Salehi, R.W.Bunce
   University of Wales — UK
   Sputter induced damage in ITO/n-GaAs Schottky barrier diodes

Monolithic Integrated V-Band TED-Oscillator

A. L. Springer, C. G. Diskus, K. Lübke, H. W. Lettenmayr, H. W. Thim

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The trend to higher operating frequencies in commercial and industrial millimeter-wave systems for radar and communication applications has stimulated research on solid-state oscillators capable of producing enough output power at these ISM-band frequencies. While rapid progress in monolithic integration technologies has led to low cost mass production of millimeter-wave systems a tunable signal source remains one of the key elements in the design of such systems. Bipolar and field effect transistors are IC-compatible but need highly sophisticated production technologies and complex circuits to meet all requirements. Two-terminal devices like Gunn and IMPATT diodes which are commonly used at millimeter wave frequencies are not suited for monolithic integration. The planar transferred electron oscillator (TEO) is a very attractive millimeter- wave signal source as new results presented in this contribution will show.

Our device the so-called FECTED (**F**ield **E**ffect **C**ontrolled **T**ransferred **E**lectron **D**evice) is a planar transferred electron device with a Schottky-gate field effect transistor replacing the ohmic cathode contact [1]. Fig.1 shows the cross sectional view of the FECTED which consists of an n-doped channel layer with three contacts applied to it: an ohmic source contact, an overlapping Schottky gate contact and a Schottky drain contact. By applying a negative bias voltage to the gate contact (with respect to the source potential) the electron injection into the drift region between gate and drain is reduced. This results in a stable high field domain which is pinned at the drain side of the gate. The frequency-independent negative differential resistance of this region is used for millimeter-wave power generation by connecting the FECTED to a microstrip open stub resonator which determines the frequency of operation of the oscillator.

Previous experiments performed with V-band MMIC-FECTED oscillators showed an output power of 0.65 mW at 54.7 GHz with an efficiency of 0.4% [1]. Since then several improvements of the oscillator circuit have been carried out leading to higher power levels with better efficiencies at higher frequencies. With shorter and narrower microstrip resonator stubs which compensate the device capacitance significantly improved results could be obtained. A slightly shortened distance from the source to its grounding via a 180° radial stub shifted the operating frequency further upwards. CW output power and efficiency achieved with this improved circuit design are 3.5mW (5.4dBm) and 0.71% at 59.7 GHz, respectively. Fig.2 shows the measured output power and the frequency of operation vs. gate-source voltage of an MMIC-FECTED-oscillator. A tuning range of up to 800 MHz with the frequency varying linearly with gate voltage can clearly be seen. The highest frequency measured with this design was 63.8 GHz with an associated power of 1 mW and an efficiency of 0.27%. Further work will concentrate on achieving maximum output power at larger negative gate voltage in order to get a wider tuning range with slowly varying output power.

This work was supported by the Austrian Science Foundation under project number P8697-TEC.

[1] A.L. Springer et. al. "*Field Effect Controlled Transferred Electron Device (FECTED) Operation at V-Band Frequencies*", Digest to the 17th European Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE'93), Parma

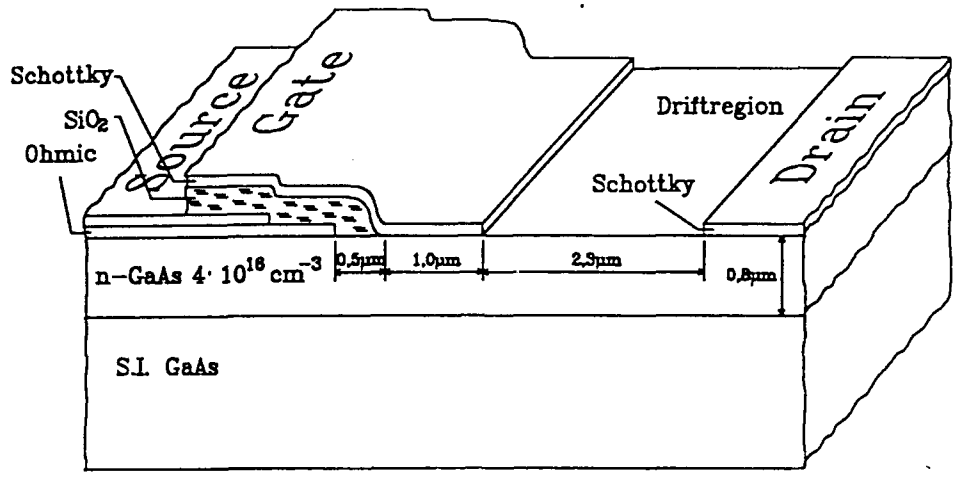

Fig. 1 Cross sectional view of the FECTED

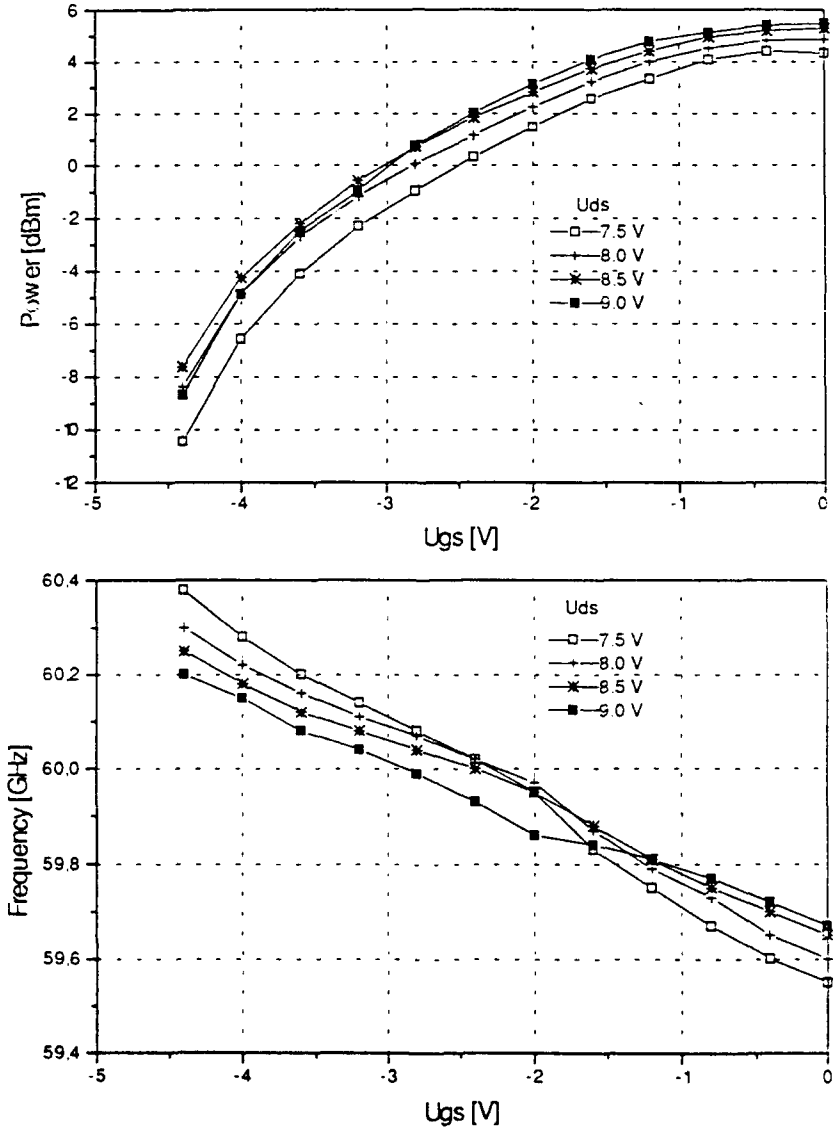

Fig.2 Power and Frequency vs. Gate-Source-Voltage of a FECTED-MMIC-Oscillator

mm-wave GaAs Impatt diodes using new encapsulation technique

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At mm-wave frequencies two-terminal devices are used in a variety of oscillator applications. With increasing frequencies the parasitic elements due to encapsulation determine more and more the oscillator behaviour. In this paper a new encapsulation technique is described which minimizes absolutely the parasitic elements and improves the heat dissipation. As active devices GaAs Impatt diodes are chosen which can operate up to frequencies well above 100 GHz. The encapsulation technique is employed for waveguide cap resonators, a type which has been applied up to the highest frequencies.

Using photoresist technology a self-supporting cap structure with three active devices (below the cap) is realized. Initial material is GaAs substrate on which the layers for the active region of the Impatt diodes (single-drift, flat-profile) are grown by MBE technique. By the help of selective etching three single devices with 20 μm diameter and a total thickness of 2 μm are realized on an integral gold heat-sink. On top the devices again cylindrical gold heat-sinks with approximately 15 μm height are grown electrolithically which carry the gold cap (also plated). The entire structure is soldered on a copper heat-sink representing the waveguide bottom of the resonator.

The design of this resonator structure with only 15 μm distance between cap and waveguide bottom is achieved by using a finite element CAD-software package.

No additional encapsulation elements like quartz stand-offs, rings, or gold ribbons are neccessary (which normally transform the active device impedance) leading to a reduction of power and efficiency as well as maximum frequency. As no stand-off material is applied the parasitic capacitance is as low as possible. The parasitic inductance of the encapsulation is determined only by the height of the conducting material on top of the devices. The whole structure is fabricated by monolithic integration which allows a precise control and high reproducibility.

The further advantage of this encapsulation technique is the improved heat dissipation which is very important for the application at higher frequencies. The dissipation of three single devices is much better than for one device with the same active area. Additionally, the gold heat-sinks on top of the devices cause a lower heat flow resistance. Therefore, the gold, respectively, copper heat-sinking technology with less expense (as compared to the one with diamonds) could be applied with success up to 100 GHz, a frequency limit which normally is achieved for GaAs Impatt diodes only with diamond heat-sinks. The maximum dc-current density for this encapsulation technique with Impatt diodes of about 13 V breakdown voltage is 30 kA/cm^2, corresponding to a maximum total dc-input power of about 3.7 W (for a temperature rise of 200 K). The devices are tested at W-band frequencies in cap resonators. Cw output power in the frequency range from 86 GHz to 100 GHz was obtained leading to an amount from 80 mW to 30 mW, respectively. These are the highest values for cw output power achieved on coppper heat-sinks in the given frequency range. The implementation of the described encapsulation technique on diamond heat-sinks will be the next step of investigation.

Design and Fabrication of a Planar THz Schottky Diode with Quasi Vertical Structure

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Abstract

We describe the design and fabrication of a planar Schottky diode applicable for THz heterodyne receiver systems. To achieve reduced parasitics, a mesa with a vertical diode (150nm epi layer, 5µm n^+ layer) is placed on a gold membrane providing the ohmic contact. The anode (1-3 µm diameter), on top of the mesa, is contacted by an air bridge to a contact pad.

The structure is making use of some advantages of the mature technology of the whisker-contacted Schottky diode concept, and, compared to different concepts of planar diodes, exhibits a reduced series resistance and a low parasitic shunt capacitance.

The analysis of the series resistance takes into account the ohmic contact resistance, the contribution of the n^+ layer and the resistance of the undepleted epi layer, considering current spreading in the epi and n^+ layers. The parasitic capacitance is calculated using a general-purpose 3-dimensional CAD finite-difference program package. Based on these capabilities we present simulations with varying dimensions and derive design considerations for low parasitics.

We discuss the different technological steps for the diode fabrication. The formation of a small sized GaAs mesa (15 µm diameter, 5 µm height), necessary for low parasitic capacitance, on top of a gold membrane (30 x 80 μm^2) is presented in detail.

18th Workshop on Compound Semiconductor Devices and Integrated Circuits
Cork, Ireland, 29 May - 1 June 1994

THz Planar Varactor Diodes Based on InAlAs/InGaAs Heterostructures

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Varactor diodes with THz cutoff frequencies are key components for generating submillimeter signals, as for example required for planetary space studies. GaAs-based whisker-contacted diodes have traditionally been used for this purpose. More recently, planar designs have been proposed to overcome the problems associated with whisker contacts. This paper presents an alternative solution which employs InP-based materials. The InAlAs/InGaAs heterostructure used in these designs provides the possibility of an enhanced C-V nonlinearity. Moreover, the InGaAs material also offers high saturation velocity and mobility, potentially resulting in a reduced equivalent access resistance (R_s) and higher cutoff frequency (f_c) relative to GaAs. The above features of the InGaAs/InAlAs design give it a potentially lower conversion loss than GaAs-based varactors. Planar technology has been developed here for these InP-based diodes and will be described.

The diode layers were grown in-house by MOCVD. Typical structures consist of a 1μm thick n+ ($5x10^{18}cm^{-3}$) InGaAs ohmic contact layer followed by a 400Å to 800Å thick (d_2) InGaAs layer and a 100Å to 200Å (d_1) $In_xAl_{1-x}As$ (x = 0.52 or 0.4) barrier layer. Although InGaAs properties were optimum at a 550°C growth temperature, a higher temperature of 650°C was selected for growing the entire structure since this minimized background doping and trap content in the InAlAs barrier layer. This layer is important for both the formation of the heterostructure and reduction of leakage currents which would have been significant for Schottky contacts directly formed on high In composition InGaAs.

The diode fabrication steps consist of a mesa etch, ohmic and interconnect metal deposition, pillar, air-bridge, and isolation etch. Unlike previous reports where anode openings are made through an SiO_2 layer which supports the air-bridge, the technology developed here employs the pillar resist for both anode definition and protection of the active areas during the isolation etch. Following anode patterning, this resist layer is then exposed, a second time, with the isolation etch mask. However, development of the isolation etch pattern is delayed until after formation of the airbridges. The isolation mask allows exposure of the pillar resist between the diode contact pad under the airbridges, while shading it over the pads and active regions. When the isolation patterns are developed, the pillar resist is also cleared from under the airbridges, thus allowing the isolation etchant to immediately attack the n+ semiconductor beneath the airbridges. Consequently, in contrast to most other planar diode processes, it is not necessary to undercut the airbridges to etch the n+ semiconductor beneath them, which should allow fabrication of diodes with much shorter airbridges.

Following processing, the InP substrate is removed and the diodes are transferred via an epitaxial lift-off process to thin (50-130μm) quartz or glass substrates. The use of quartz or glass as the substrate decreases pad capacitance and eases dicing because, when sawed, glass and quartz show reduced chipping relative to InP. When glass is used, it is etched completely off in BHF after mounting the diode, thus reducing pad capacitance further.

These diodes showed minimum leakage of $292\mu A/cm^2$ by employing an $In_{0.40}Al_{0.60}As$, 200Å thick barrier. The largest C_{max}/C_{min} ratio achieved was 2.55 and the highest cutoff frequency approached 2.4THz using 1μm diameter anodes.

Work Supported by NASA Contract NAGW-1334 and URI (DAALO3-92-6-0109)

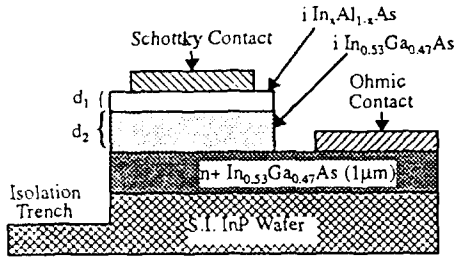

Figure 1. Schematic cross-section of the InP-based heterojunction varactor diode.

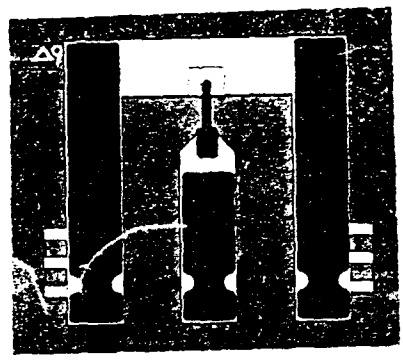

Figure 3. Photograph of fabricated InAlAs/InGaAs varactor. The Schottky anode is connected to the anode pad via an airbridge. This pad layout allows on-wafer microwave probing.

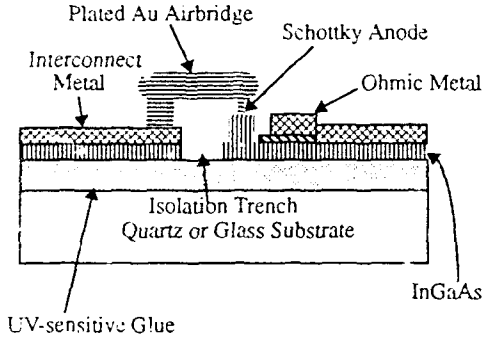

Figure 2. Side view of InAlAs/InGaAs varactor diode that had its InP substrate replaced with glass or quartz. The glass (or quartz) substrates can range from 50 to 130μm in thickness. The adhesive used to attach the diodes to their new substrate is cured via UV exposure.

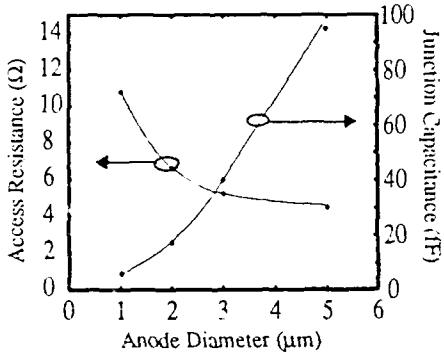

Figure 4. Impact of anode diameter on access resistance (R_s) and junction capacitance at zero bias ($C_j(0V)$). Here, d_1 = 200Å, d_2 = 800Å, and x = 0.52. For the 1μm anode diameter diode, the cutoff frequency is 2.37THz, $C_j(0V)$ is 6.2fF, and R_s is 10.8Ω.

Epitaxial Diamond Schottky Diode on p^+ - Substrate

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Diamond Schottky diodes are attractive for high temperature, microwave and power applications. However the deep energy level (380meV) of the boron acceptor in lightly doped diamond ($<10^{17}cm^{-3}$) causes carrier freeze-out at R.T., which in turn gives rise to a severe parasitic series resistance rendering the device insulation at lower temperature. It is therefore essential to employ a thin active epitaxial layer on a p^+-substrate. Due to the low activation energy of the such a substrate (50meV) its resistivity ($\approx 100\Omega cm$) is 3 orders of magnitude lower than the resistivity of natural, boron doped diamond.

Epitaxial diodes (Fig.1) are fabricated by growing a 1µm thick diamond layer on top of the [100]-oriented 1 mm thick substrate by PECVD. The diode area ($\approx 10^{-4}$ cm^2) is defined by the Au-Schottky metal. The ohmic contact on the back-side of the substrate is made by alloyed tantalum. The doping concentration of the epitaxial layer estimated by CV-measurements is $1.1 \times 10^{17} cm^{-3}$.

The I/V-characteristic of a typical diode is shown in Fig.2 for temperatures ranging from 50°C to 500°C. At forward bias an exponential I/V-behavior is observed over more than 3 decades of current. The current densities reaching more than $10^3 A/cm^2$. Analysing this region in detail, a temperature dependent ideality factor is extracted ranging from n = 1.7 at 50°C to n = 1.1 at 500°C. Thus the diode behavior improves with temperature.

These low ideality factors allow to extract a meaningfull barrier height. It was calculated from the upper part of the Richardson plot, where the thermal emission dominates, and yields $\Phi_{b(I/V)} = 1.55$ eV.

The series resistances were extracted from the I/V-characteristics at high forward bias. Fig.3 shows the differential diode resistance at forward and reverse bias vs. temperature. At high forward bias (-6V) and low temperature the resistance of the epitaxial layer dominates the series resistance, displaying the activation energy of moderately doped diamond films (380 meV). However, above 150°C the substrate resistance, displaying the activation energy of the substrate, becomes the limiting element. Thus, the series resistance is small ($<20\Omega$) above 150°C, which is also the envisioned temperature range of operation for the diode.

The small series resistance enables a current rectification ratio of 10^5 at ±2 V. This ratio is however now limited by the reverse bias leakage current, which does also rise with temperature. Its temperature dependence can also be described by an activation energy of approx. 380 meV. No breakdown of the diamond material is observed up to high reverse current levels approaching the forward levels.

The series resistance of the diode can be further optimized by tailoring the epitaxial layer thickness and doping profile.

Fig. 1

structure of the
p/p$^+$ - Schottky diode

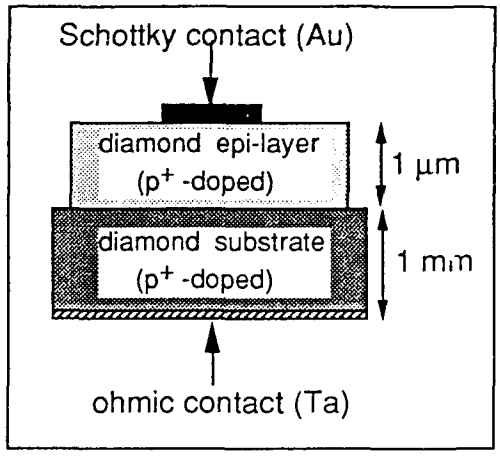


Fig. 2

I/V- characteristics of the
p/p$^+$ - Schottky diode
at different temperatures

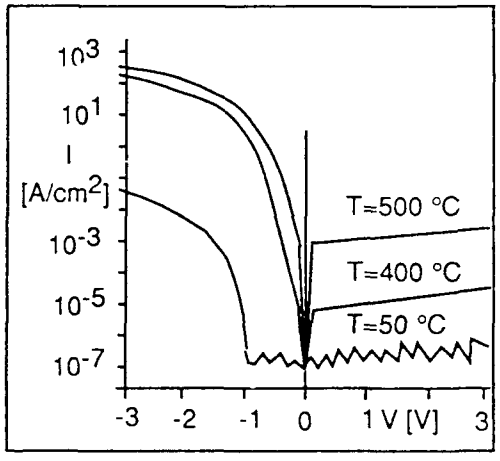
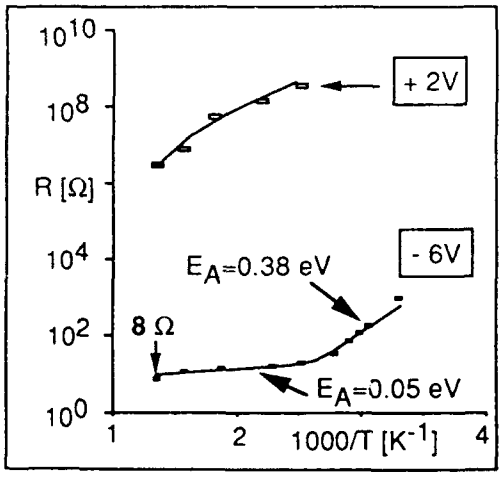


Fig. 3

temperaure dependent
differential resistance of the
p/p$^+$ - Schottky diode at
forward (-6V)
and reverse bias (2V)
$R_{on}/R_{off} = 10^5 - 10^6$
$A=5x10^{-5}cm^2$



Hot electron noise temperature in an n-type GaAs channel at fields over 100 kV/cm

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Electric field is known to exceed 100 *kV/cm* in a submicron region of a MESFET channel at its drain end [1]. Electrons are extremely hot there, and their contribution to excess microwave noise is quite important for power-noise and speed-noise trade-offs.

Because of limited knowledge of band structure and scattering at elevated energies, calculations of hot electron noise at extremely high electric fields lack accuracy, and experimental investigation seems to be the main source for obtaining reliable information. However, to our knowledge, no experimental data on hot electron noise in an *n*-type GaAs channel at fields over 100 *kV/cm* has ever been reported.

We measured hot electron noise temperature at 10 *GHz* frequency at room temperature. Samples of *n*-type GaAs were Si-doped (10^{17} cm^{-3}) ungated channels with two ohmic electrodes (n^+- n - n^+ structures). The channel length was L=0.2μm to simulate the submicron high field region in a MESFET channel. Pulsed dc voltage was applied in a low duty cycle. The pulse duration was chosen to be 200 *ns*, i.e. short enough to avoid thermal breakdown at the extremely high fields.

The main results on hot electron noise temperature T_n are illustrated in Fig.1. The noise temperature reaches 20 000 *K* at UL=100 *kV/cm* field and tends to saturate at the higher fields. The noise source with a steep increase of T_n at 0.5 *V* is known to arise from the intervalley Γ-X transfer [2]. It is important that the upper valley occupation never tends to unity at very high fields in a submicron channel: when the hot electrons (present in the upper valleys) leave the channel, the cold electrons immediately enter its opposite end into the Γ-valley.

The exponential increase of T_n at fields over 200 *kV/cm* (Fig.1) is accompanied by a steep increase of current and dissipated dc power (Fig.2); this is expected to arise from impact ionization. Note, that the noise starts increasing at an essentially lower field as compared to the impact breakdown taking place at 300 *kV/cm*. This prooves the noise to be a useful tool for an "early diagnostics" of the breakdown.

The ratio of the hot electron noise power to the dissipated power can be used to discuss power-noise trade-off.

[1] G Zandler and P Lugli. In: *Proceedings WOCSDICE 92*.
[2] V Bareikis et al. *Solid State Electronics* **32**, 1647, 1989.

Experimental Results. Power transistors have been fabricated with such epitaxial structures. They have demonstrated a maximum current drive between 600 and 650 mA/mm with a drain-source breakdown voltage between 10 and 12 V (see figure 3). At 2, 10 and 20 GHz a saturated output

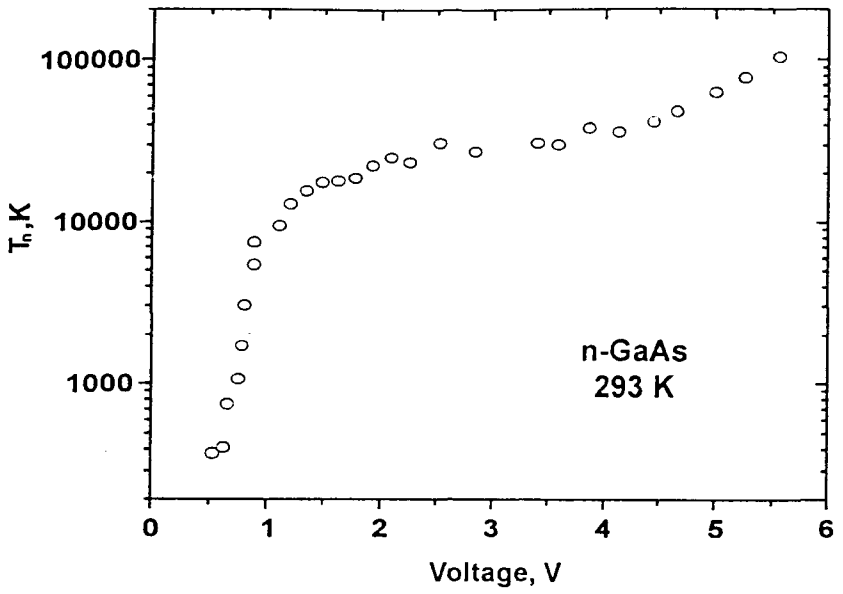

Fig.1. Experimental voltage dependence of hot electron noise temperature in a 0.2 μm channel of n-type GaAs

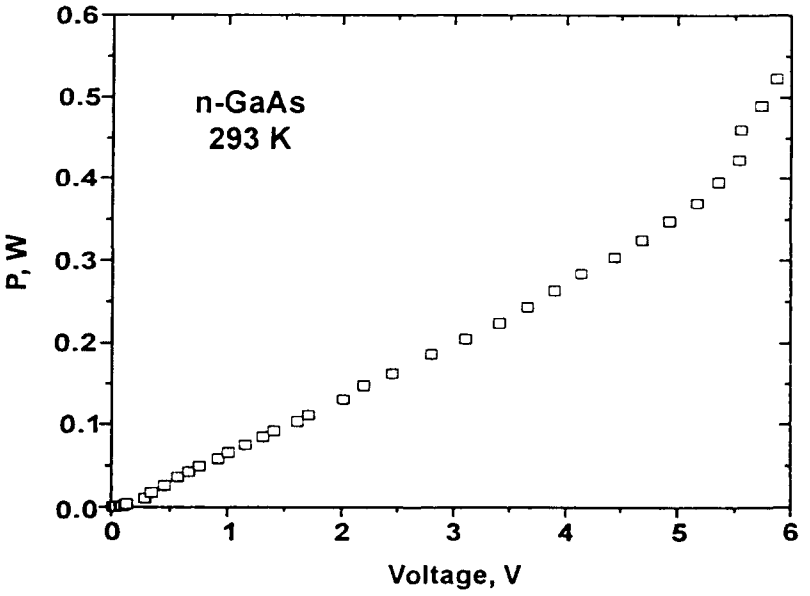

Fig.2. Dissipated pulsed dc power vs pulsed dc voltage for a 0.2 μm channel of n-type GaAs

SPUTTER-INDUCED DAMAGE IN ITO/n-GaAs SCHOTTKY BARRIER DIODES

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ABSTRACT

Transparent conducting oxides are used as a contact material for electro-optical applications due to their interesting combinations of properties namely high visible transparency (80-90%) and electrical conductivity. One of the most important potential uses is to replace the metal on a Schottky barrier, thus forming a 'window layer' on the semiconductor. A great variety of techniques of deposition have been reported for depositing these films including sputtering, chemical vapour deposition, electron-beam and thermal evaporation[1,2]. There are however few reports available on the effect of these deposition techniques on the diode electrical and optical performances. This paper reports our studies on the effect of sputter induced damage on Indium Tin Oxide(ITO)/n-type GaAs Schottky diodes.

Schottky barrier diodes were fabricated by sputter deposition and reactive thermal evaporation techniques. The source material for the ITO is an Indium Tin Oxide alloy (90% In - 10% Sn). n/n^+ GaAs material with doping concentration ($N_d = 9 \times 10^{24}$ m^{-3}) was used. Au-Ge(Ni) Ohmic contact were applied to the n^+ GaAs material. The samples were sputter etched for 5 minutes prior to the deposition of the ITO. The diodes were characterised by Current-Voltage(I-V), Current-Voltage at different temperatures (I-V-T), Capacitance-Voltage (C-V) measurement and Thermally Stimulated Current (TSC) measurements.

Thermal stressing of these diodes showed that sputter deposited diodes begin to degrade at lower temperatures compared to thermally evaporated diodes. This is attributed to the effect of induced damage on the GaAs. The sputter induced damage on GaAs is known to cause barrier height lowering and to induced a donor-like defect near the surface region[3].

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Session 7: Integrated devices

Chair: F. Fantini (University of Parma)

1 **J.Würfl**, K.H.Rooch, S.Thierbach
Ferdinand Braun Institute, Berlin Germany
Process technology for high temperature GaAs based integrated circuits

2. **C.Lanzieri**, M.Peroni, A.Cetronio
Alenia Italy
Self aligned process for high yield, low cost GaAs monolithic microwave integrated circuits

3. **G.Schweeger**, R.Dolt, J.Stöcker, C.Lang, K.Fricke, H.L.Hartnagel
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GaAs sensors for automotive applications

Process Technology for High Temperature GaAs-based Integrated Circuits

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Compound semiconductors based on GaAs exhibit a variety of interesting material properties that make them suitable for many device applications. The high energy bandgap of GaAs together with the excellent high frequency properties of the material favours applications in microwave devices operating at high ambient temperatures up to 350°C. In this paper we will present a MESFET technology for the fabrication of devices that are specially developed for continuous, reliable operation at high temperatures. Additionally the performance of high temperature microwave circuits, fabricated by utilizing this technology, will be discussed.

The high temperature MESFET technology is based on highly stable ohmic- and Schottky contacts employing metallizations that contain reactively sputtered WSiN diffusion barriers. All passive elements such as transmission lines, interconnections or thin film resistors (sputtered NiCr films) are completely encapsulated by using PECVD SiN_x deposition techniques. Multiple implantations of O^+-ions at different energies ensure an effective isolation of the active regions, even at very high temperatures. Drain/source leakage currents at high temperatures are significantly reduced due to the use of GaAs epitaxial MESFET wafers with AlAs/GaAs superlattice buffer layers.

MESFETs, fabricated by utilizing this technology, have been optimized to match the requirements for continuous operation at high temperatures. A physical device simulation program was applied to find out the optimum dimensions of the active channel and to optimize breakdown condition and on/off ratio of the transistors especially in the view of high temperature operation. Based on these simulations, MESFETs with 0.5 μm gate length have been fabricated. The devices were operated between -196°C (liquid nitrogen) and 300°C - a temperature range of about 500°C. In this range of temperature the variations of saturation current and transconductance are less than 15%. The typical transconductance is about 280 mS/mm at room temperature.

Self-Aligned Gate Process for High Yield, Low-Cost GaAs Monolithic Microwave Integrated Circuits

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Abstract

As we approach the stage of highly integrated, multifunctional, and mixed analogue-digital circuits, a fully ion-implanted, self-aligned GaAs MESFET technology with planar structure is advantageous because the same fabrication process can be used for all the necessary devices. Not only, it is foreseen that in the near future this technology will come to the forefront of GaAs MMIC fabrication because less critical than the present "recessed-gate" technology and thus ideal for addressing the growing demand of moderate to low-cost MMIC's for both consumer and professional electronics applications.

In this work we will outline a self-aligned ion-implantation technology which eliminates all the critical steps (i.e. gate length, recessing, lift-off, etc.) of MESFET fabrication. Said technology is based on a WN/Au gate metallisation which can withstand the high temperature (850°C for 30 seconds) post-implant annealing cycle without degradation and interdiffusion.

The SAGFET process is based on Si and C ion-implantation for active channel formation and highly selective, low damage plasma etching to produce "T-shaped" WN/Au gate structures with effective gate length controllable in the range 1 to 0.3 μm.

The devices fabricated with this technology (i.e. low-noise and power) yield very good on-wafer uniformity and high technological yield with preliminary performances already comparable with recessed-gate devices.

DR-026/94

GaAs sensors for automotive applications

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Introduction

More and more conventional sensors are replaced by smart sensors based on semiconductor circuits. However, when it comes to high-temperature applications or when sensors are to be integrated with microwave or optoelectronic circuits silicon rapidly meets limitations. GaAs has not only advantages in these aspects but in contrast to silicon it is a piezoelectric material so that pressure sensors are feasible and it also has a higher carrier mobility which is of advantage e.g. in magnetic field sensors.

The automotive industry is pushing for an increased use of sensors both to reduce fuel consumption maintaining at the same time the car's performance and to enhance the passenger's security. We want to present here two examples where the use of GaAs sensors is advantageous for the use in automotive electronics.

Piezotransistor for measuring the pressure in a combustion chamber

The precise knowledge of the pressure development in a combustion chamber would make it possible to control fuel injection time and ignition time in order to have less pollution, less fuel consumption and yet a maximum output power. In research laboratories watercooled piezoelectric ceramic sensors are used of which the output signal has to be coupled to a rather expensive and sensible charge amplifier.

Fricke [1] has shown that the transversal piezoelectric effect in (100)GaAs can be used to measure the pressure in the combustion chamber. Using the piezoelectrically generated carriers to control the gate of an integrated MESFET we have an active device of which the voltage output is great enough to be amplified by conventional circuits. GaAs has furthermore the advantage that a special water cooling of the sensor is not necessary as long as the temperature of the sensor stays below 300°C. Such a sensor could then be built into any car engine for better control of the combustion process.

We present the measuring principle, a first realisation and the pressure and temperature dependence of such a device.

Split-drain FET for magnetic field sensors to be used in car tires

The passenger's security largely depends on a perfect tire-road adhesion circle. This can be measured via the three-dimensional deformation of the tire's studs. In laboratory experiments a small magnet is vulcanised into the stud and its position measured with magnetic field sensors on the inside of the tire. The use of GaAs sensors would make it possible to miniaturise the sensor so that magnet and sensor can be integrated in the stud.

We compare different GaAs based magnetic field sensor, namely a differential Hall cross sensor and a split-drain field effect transistor as proposed earlier, e.g. [2]. The gate voltage can be used to compensate for temperature dependence and for asymmetry in the FET. Also a two-dimensional position sensor based on split-drain structures is proposed. It is obvious that 2-DEG structures with their enhanced carrier mobility will still get better results [3]. We will discuss the possible improvements.

Ultimately these structures have to be integrated with oscillators and/or modulators, so that a wireless transmission of the signal to a signal processor in the car will be possible.

Acknowledgements

The authors wish to thank the Deutsche Forschungsgemeinschaft for the funding of the project under SFB 241.

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Session 8: Optical Devices

Chair: D. Pavlidis (University of Michigan)

1. **John G. McInerney** (Invited)
   University College Cork — Ireland
   Coherent high -power semiconductor lasers

2. W.Batty, **D.W.E.Allsopp**
   University of York — UK
   Theoretical large improvement in phase shift efficiency of MQW Mach Zender optical modulators utilising shaped quantum wells

3. **Sean S. O'Keefe**, G .Martin, D.W.Woodard, W.J.Schaff, L.F.Eastman
   Cornell University — USA
   CPW transmission lines on polycrystalline diamond substrates for a 4x4 VCSEL array

4. I.B.Petrescu-Prahova, M.Buda, W van der Vleuten, F.Karuta, **T.G. van de Roer**
   Eindhoven — Romania/Netherlands
   Design of a 1W single filament laser diode

5. **L.F.Eastman**, J.Burm, K.Litvin, W.J.Schaff
   Cornell University — USA
   Optimised MSM photodetectors

6. **C.J. van der Poel** (Invited)
   Philips — Netherlands
   Progress in strained layer quantum well lasers

7. **Aidong Shen**, M.Maier, E.C.Larkins, H.Schneider, B.Dischler, R.Dian, M.Baeumler, J.Forker, W.Rothemund, W.Janz, J.D. Ralston
   Fraunhofer Institute — Germany
   Beryllium migration in strain relaxed InGaAs/GaAs MQW pin photodetectors grown by MBE

8. J.L.Sánchez-Rojas, A.Sacedón, **E.Muñoz**, E.Calleja, F.Calle, F.González-Sanz, D.R.Harken, X.R.Huang, D.S.McCallum, A.N.Cartwright, A.L.Smirl
   University Politecnica Madrid, University of Iowa — Spain/USA
   Conduction band Engineering and time response in piezoelectric [111] MQW photodiodes

9. **J.J. Pérez-Camacho**, J.Anguita, F.Briones
   CNN Madrid — Spain
   GaInSb infrared photodiodes grown by MBE

10. **A.Morrison**, J.D.Lambkin, E.O'Sullivan, S.Fahy
    NMRC, University College Cork — Ireland
    Design of a multiquantum barrier using an extended effective mass model to include the effects of Γ-X mixing

Coherent High-Power Semiconductor Lasers

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Semiconductor injection (diode) lasers are among the most versatile and usable of all laser types, combining compactness, ruggedness, high efficiency and ease of pumping. They are available as single devices in powers ranging from mW to ~1W and in incoherent arrays to kW. Here we discuss which application require coherence and which simply raw power, and we will describe the two most promising high power semiconductor laser structures which can combine multiwatt powers with high spatial coherence (ideally in a single transverse mode): unstable resonator devices and master oscillator-power amplifier (MOPA) configurations. Design and fabrication issues will be addressed.

THEORETICAL LARGE IMPROVEMENT IN PHASE SHIFT EFFICIENCY OF MQW MACH ZEHNDER OPTICAL MODULATORS UTILISING SHAPED QUANTUM WELLS

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Interferometric techniques provide a near ideal means of modulating optical intensity at high data rates because chirp can be controlled. When operated in push-pull mode, the change in absorption with refractive index variation introduced in one arm of an integrated Mach-Zehnder (MZ) interferometer can be offset by an almost equal and opposite change in the other, resulting in negligible chirp. Increases in the electric field sensitivity of relevant electro-optic effects can give rise to reduced device lengths (hence higher electrical bandwidths) or lower operating voltages, depending on the system requirement. In essence stronger electro-optic effects give rise to improvements in the phase shift efficiency (PSE) of MZ modulators.

The Quantum Confined Stark Effect (QCSE) in semiconductor quantum wells has been shown to produce a strong associated refractive index change that is quadratic with electric field [1]. However, harnessing this electrorefractive effect for efficient MZ modulator operation is not straightforward for the following reasons. First, the optical filling factor of an MQW waveguide core is usually less than half that of an equivalent bulk layer, giving rise to a need to enhance the total refractive index change per unit applied field by at least a factor two. Second, the oscillatory, bipolar nature of the differential absorption spectrum associated with the QCSE gives rise to contributions of different sign from successive energy ranges in the Kramers-Kronig transformation. As a consequence a strong QCSE does not necessarily yield large concomitant refractive index changes at a given incident wavelength.

Two strategies have been proposed for enhancing QCSE-related electrorefraction. Zucker and co-workers have demonstrated that prebiasing an GaAs/AlGaAs MQW MZ modulator with a DC voltage > 20 V improves the PSE [2]. Alternatively it has been shown theoretically that the differential absorption spectrum can be engineered to be essentially unipolar over a large energy range by shaping the quantum well, to produce a more favourable Kramers-Kronig transformation [3,4]. In this paper it shown that, by using symmetric stepped quantum wells (SSQWs), large theoretical improvements in the PSE of MZ modulators can be obtained.

The inset of figure 1 shows schematically an SSQW. The lower part of figure 1 compares the calculated spectral dependence of absorption of a GaAs/AlGaAs SSQW with that of an equivalent square quantum well (SQW) at applied electric field strengths of 0 and 4 V/μm. The SSQW comprised a 2 nm GaAs notch placed centrally in 42 nm wide $Al_{0.2}Ga_{0.8}As$ outer well, surrounded by $Al_{0.4}Ga_{0.6}As$ barriers.

Absorption in the SSQW is characterised by the collapse of the ground state exciton peak at an applied electric field of 4 V/μm. The exciton decays as the conduction band quantum well in the GaAs notch couples with the triangular quantum well formed at the interface between the outer $Al_{0.2}Ga_{0.8}As$ well and the barrier in the up-field direction, thus allowing the electron to tunnel from

the GaAs inner well. This process produces a unipolar differential absorption spectrum that yields, on Kramers-Kronig transformation, a large decrease in the refractive index. The upper part of figure 1 compares the refractive index change that results for the field increase from 0 to 4 V/μm for the SSQW and the equivalent SQW. In the detuned wavelength range in which MZ modulators are operated (ie below the absorption edge) the SSQW gives a much larger refractive index change.

In the paper other structures, notably InP/quaternary devices for 1.55 μm wavelength applications, will be considered and these results, together with their implications for PSE, will discussed.

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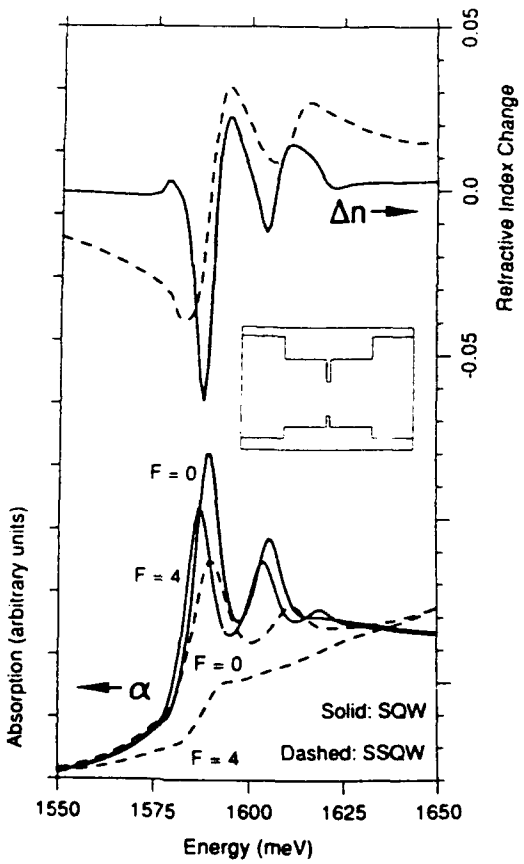

Figure 1 *Lower: absorption spectra for the SSQW (dashed) and its equivalent SQW (solid). Upper: the sepctral dependence of the corresponding refractive index changes for electric fields of 0 and 4 V/μm.*

CPW Transmission Lines on Polycrystalline Diamond Substrates for a 4x4 VCSEL Array

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Polycrystalline chemical vapor deposition (CVD) diamond substrate production has evolved very rapidly in the past few years and a new application of diamond heat sinks is presented. CVD diamond's properties of high electrical resistivity and high thermal conductivity make it an ideal substrate for high power density microwave and high speed optoelectronic applications. In this work, coplanar waveguide transmission lines were patterned on CVD diamond substrates. Insertion loss to the inside feed points of a 4x4 array of vertical cavity surface emitting lasers (VCSEL) is less than 0.1dB up to 30 GHz. Fabrication techniques, microwave characterization of CPW transmission lines on CVD diamond substrates, and application to a densely packed 2-d array of VCSELs for high speed parallel optical communications links will be presented.

DESIGN OF A 1 W, SINGLE FILAMENT LASER DIODE

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Abstract

A design of a high power laser structure is presented which is based on an increase of the cavity length as well as a maximization of the stripe width. This requires a low value for the modal attenuation coefficient (about 1 cm^{-1}) and a low optical confinement factor (less than 1 percent). A model is presented from which the modal gain, the confinement factor, the active region thickness, the stripe width, the length and the reflection coefficients can be calculated. A variant for all design parameters needed to reach 1 W emission in the fundamental lateral mode is given. These values are used to design the epitaxial structure.

Based on these design specifications an epitaxial structure has been grown by the MBE facility of Eindhoven University (group of Semiconductor Physics) and processed in the group of Electronic Devices. The first results are encouraging: the 0.9 W level is reached in pulsed operation and the modal attenuation, obtained in the usual way by comparing lasers of different lengths, shows a value of 1.5 cm^{-1}.

Optimized M-S-M Photodetectors

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The optimized frequency response and quantum efficiency of M-S-M photodetectors are presented. The charge carrier transit time and the RC time are made equal, and the aperture diameter is a variable. The frequency response is about 60 GHz for a 20 μm diameter, where the adjacent fingers are centered about .6 μm apart, and the frequency response depends reciprocally on the aperture diameter. This yields an optimum number of metal fingers, of 33. A thin GaAs absorbing layer, a Bragg reflection stack underneath, and an AlGaAs window layer on top, are used. All the incident light at ~ .80 μm wavelength, is absorbed, and no surface recombination results. A method of eliminating the reflection of polarized light from the metal fingers will also be presented. This will allow nearly 100% quantum efficiency, and frequency response in the range of 50 - 200 GHz, depending on the aperture, and resulting finger, designs.

This research is supported by Rome Laboratories and Hughes Research Laboratory.

Progress in Strained Layer Quantum Well lasers

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Whereas only 5 years ago the application of strain in semiconductor diode lasers was considered detrimental to laser performance and therefore to be avoided at all times, nowadays many modern commercial diode lasers, modulators and amplifiers employ and benefit from active-layer structures with a deliberately built-in controlled amount of tensile or compressive strain.

When properly dimensioned, the changes in bandstructure induced by the built-in strain [1,2] can significantly improve the laser characteristics and add new freedom in the choice of lasing wavelength and light polarization.

As an illustration, figure 1 shows the wavelengths that can be adressed by applying strained layer QW's in InGaAs/GaAs and GaAsP/GaAs materials. At a QW width of 90 Å and with the strain varying from -1.0 % tensile to +1.2 % compressive a wavelength span of about 200 Å is covered. Strained-layer diode lasers at the previously unadressable wavelength of 980 nm have become of commercial importance as reliable pump sources in Er doped fiber amplifiers for long-distance 1.5 μm optical communication systems.

In figure 2, we have collected recent results on the effects of strain and temperature on the threshold current of broad-area strained layer QW diode lasers at the visible, near-infrared and infrared wavelengths, as fabricated by OMVPE. As is obvious from the figure, the effects of strain on threshold current can be quite large. The improvement differs for each wavelength range and can be traced back to changes in carrier loss and optical loss mechanisms in the subsequent material systems. Using the regions of optimal strain of figure 2, narrow stripe laser devices with submA threshold current, high differential efficiency and with reliable high-power output have now been realized and these devices are used in the most advanced commercial visible and telecommunication lasers.

Furthermore, by elegant manipulation of both tensile and compressive strained QWs in a single active layer, see figure 3, the strain dependance of the light polarization can be used for TE/TM polarization control. In this way a polarization insensitive 1.3 μm chip amplifier with a fiber-to-fiber gain of $\geq$ 24 dB has been obtained and successfully applied as optical preamplifier in a 10 Gb/s transmission experiment.

This paper will review some of the origins of the above results, identify areas where additional understanding is needed and discuss future trends and applications in this rich and rapidly evolving research field.

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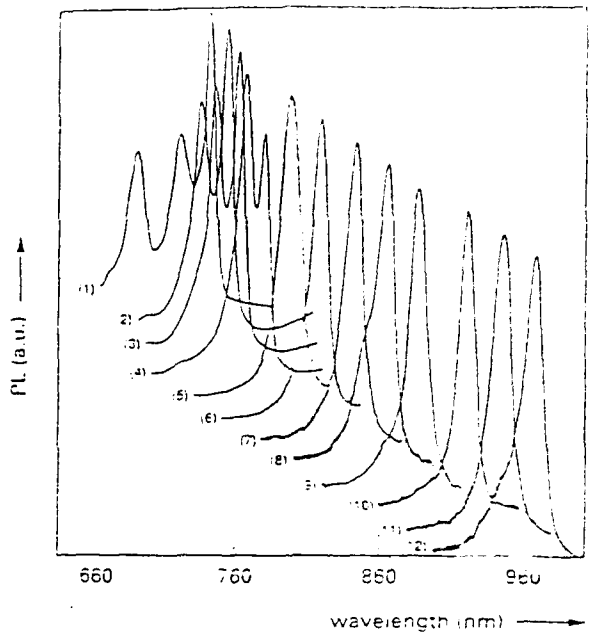
Figure 1

Room-temperature Photo-Luminescence spectra of GaAsP/GaAs and InGaAs/GaAs strained-layer QW diode laser structures with a QW thickness of 90 Å at variable amount of strain.



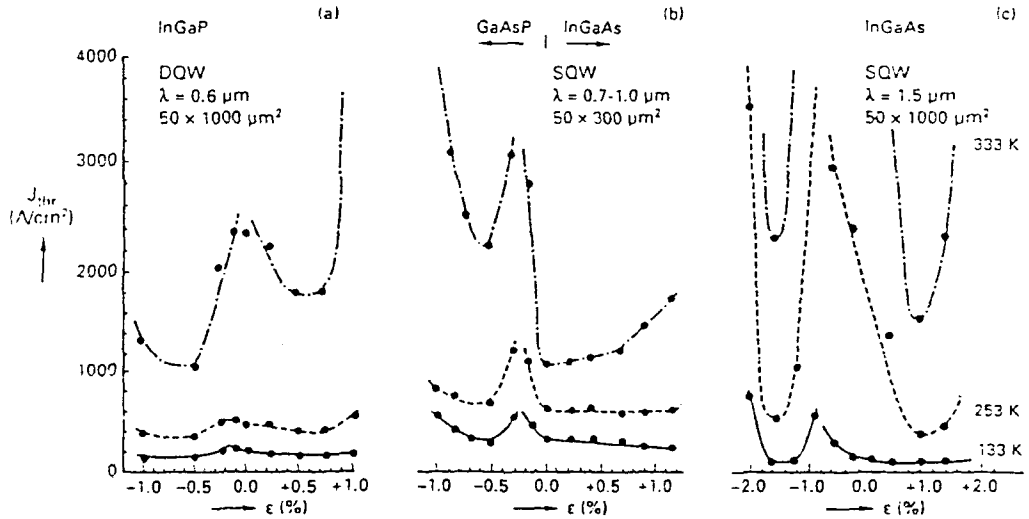


Figure 2

Threshold current density as a function of temperature and strain for strained layer QW devices in the (a) visible, (b) near infrared and (c) infrared wavelength ranges.

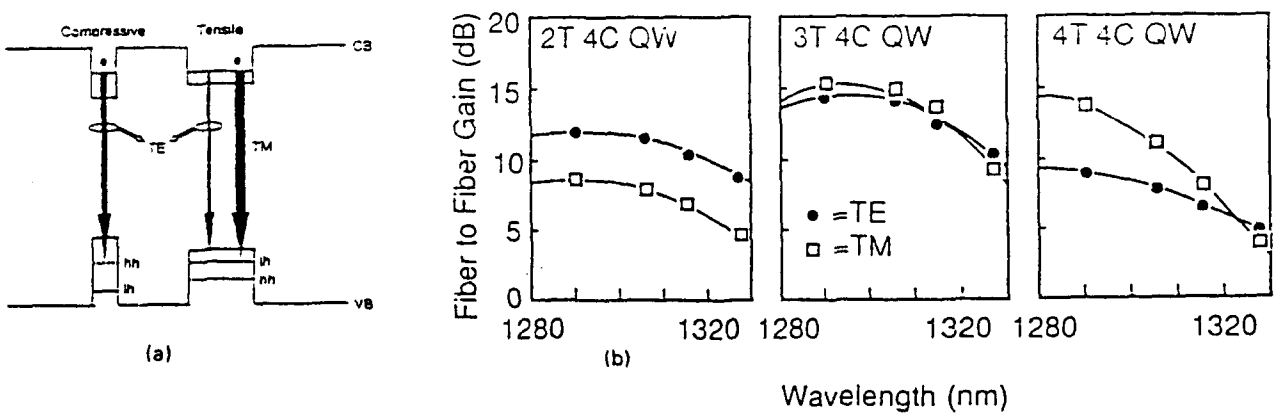


Figure 3

Principle (a) and fiber-to-fiber gain (b) of 1.3μm strained layer optical amplifiers as function of active layer structure

Beryllium migration in strain-relaxed InGaAs/GaAs MQW p-i-n photodetectors grown by MBE

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Strained-layer InGaAs/GaAs QW structures have been utilized successfully for the fabrication of a variety of optoelectronic devices. We have recently demonstrated $In_{0.35}Ga_{0.65}As$/GaAs MQW lasers with record direct modulation bandwidths exceeding 30 GHz at wavelengths of 1.0-1.1 μm[1], in a device structure suitable for monolithic integration with GaAs-based MODFETs[2], as well as a variety of $In_yGa_{1-y}As$/GaAs MQW waveguide modulators and switches[3]. We have also demonstrated strain-relaxed $In_yGa_{1-y}As$/GaAs MQW p-i-n photodetectors[4] as promising high-speed detector candidates, compatible with the above lasers. To match the operating wavelength of the lasers and to obtain efficient absorption, it is necessary to increase both the indium content of the QWs and the number of QWs in the detector active region, resulting in increased strain relaxation. At the same time, it is necessary to use a heavily p-doped GaAs cap layer to minimize the contact resistance of the device. Thus, the effect of the misfit dislocation network on the incorporation and redistribution of dopant impurities is particularly important. Although Be redistribution and migration in GaAs/AlGaAs has been studied[5], the behavior of heavy Be doping in strain-relaxed InGaAs has received little attention. We have studied the incorporation of Be in p-i-n detectors with strain-relaxed $In_yGa_{1-y}As$/GaAs MQWs ($0.30 \le y \le 0.45$), using optical absorption, secondary ion mass spectrometry (SIMS), photoluminescence (PL), differential interference contrast microscopy (DICM) and PL microscopy (PLM). Interstitial Be is shown for the first time to interact strongly with the misfit dislocation network, seriously degrading the MQW excitonic absorption. Suitable modifications to the cap layer doping profile are shown to greatly reduce such detrimental dopant/dislocation interactions. These results are also important for optical modulators fabricated from strain-relaxed $In_yGa_{1-y}As$/GaAs MQWs[3,6].

Three series of $In_yGa_{1-y}As$/GaAs p-i-n detectors were grown by MBE with 5.7 nm QWs, maintaining a constant MQW thickness of 350 nm. In the first series of five detectors, the In fraction was fixed at y=0.35 and the number of QWs was varied from 6 to 41. In the second series, the number of QWs was fixed at 12 and y was varied from 0.35 to 0.45. In both series, a GaAs:Be layer, nominally composed of 300nm ([Be] = $8x10^{18}$ cm^{-3}) GaAs and 200 nm ([Be] = $8x10^{19}$ cm^{-3}) GaAs, was grown directly on top of the MQW structure. In the third series, the MQW structure is the same as in the first series, but the p-region was nominally composed of 200 nm GaAs ([Be] = $2x10^{18}$ cm^{-3}), 217 nm GaAs ([Be] = $8x10^{18}$ cm^{-3}) and a 83.4 nm GaAs ([p] = $8x10^{19}$ cm^{-3}) cap layer. In addition, 50 nm of undoped GaAs was added between the p-type region and the MQW.

Good excitonic absorption is essential both for p-i-n photodetectors and for optical modulators. However, near infrared aborption measurements on the first series of samples show a very weak excitonic absorption in the 1.0-1.1 μm range, which decreases rapidly as the number of QWs increases. As seen in Fig.1, the excitonic absorption has nearly disappeared in the 20 QW sample. SIMS profiles on these samples show that Be has diffused into the MQW structure at concentrations sufficient to bleach the excitonic absorption. Fig. 2 shows the SIMS profiles of four samples in the first series, with 12, 20, 30 and 41 QWs. The Be concentration in the MQW region increases from ~$5x10^{12}$ cm^{-2} for the 6 QW detector (not shown) to ~$6x10^{14}$ cm^{-2} for the 41 QW detector. At the same time, the penetration depth of the Be increases from about 10 nm to about 350 nm. The SIMS profiles of the second series are shown in Fig. 3. As the indium fraction increases from y=0.35 to y=0.45, the Be concentration increases from $1.0x10^{14}$ cm^{-2} to $8.0x10^{14}$ cm^{-2} and the penetration depth increases from 55 nm to 385 nm. DICM and PLM measurements show that only the 6 QW structure with y=0.35 is unrelaxed. Thus, it appears that the diffusion of Be into the MQW structure is strongly enhanced by the misfit dislocation network and becomes more severe as the degree of lattice relaxation increases. At concentrations above 10^{19} cm^{-3}, Be begins to incorporate interstitially[5]. In the third series of samples, the modification to the cap layer doping reduce the total Be concentration only by a factor of 2, but the Be in the active region decreases by up to two orders of magnitude. This is a clear indication that the diffusion of Be interstitials along the dislocation network is ultimately responsible for the bleaching of the excitonic absorption.

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Figure 1: Absorption spectra from the first series of detectors with 6, 12 and 20 QWs. The decrease in absorption with increasing number of QWs reflects the absorption bleaching due to Be diffusion into the strain-relaxed MQW structure.

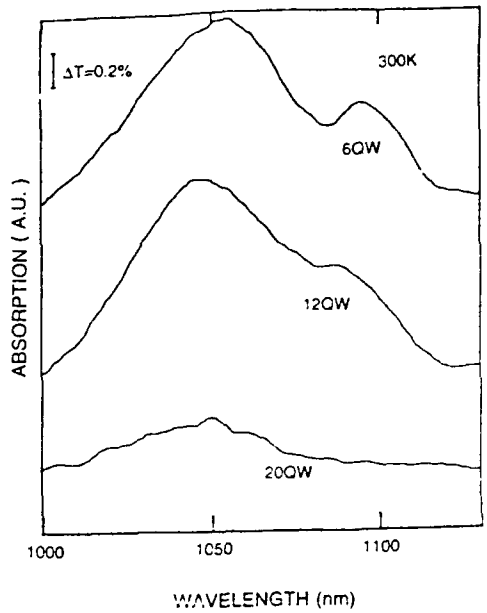


Figure 2: Be doping profiles obtained with SIMS from samples in the first series of detectors with 12, 20, 30, and 41 QWs. As the number of QWs increases, the amount and depth of Be diffusion increases dramatically.

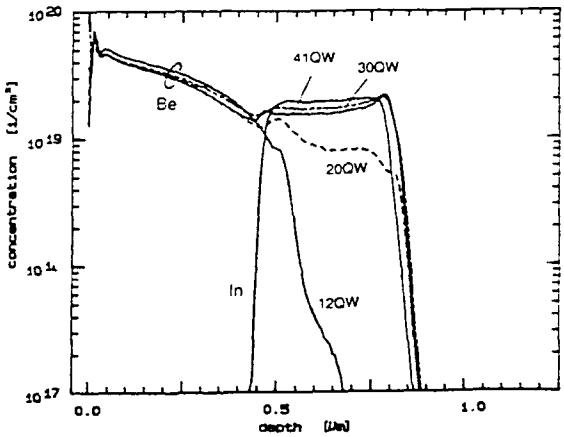
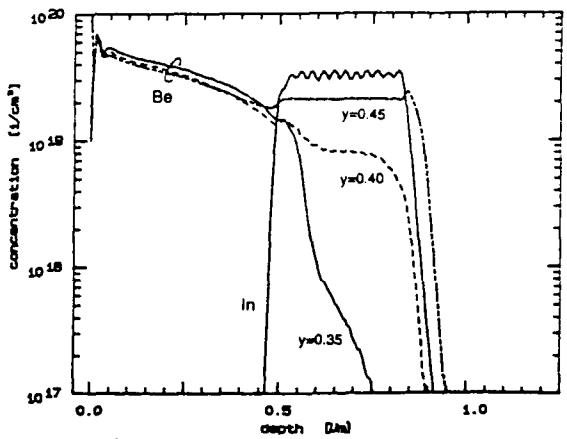


Figure 3: Be doping profiles obtained with SIMS from samples in the second series of detectors with y=0.35, 0.40, and 0.45. As the indium concentration in the QWs increases, the amount and depth of Be diffusion also increases dramatically.



CONDUCTION BAND ENGINEERING AND TIME RESPONSE IN PIEZOELECTRIC [111] MULTIPLE QUANTUM WELL PHOTODIODES

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The strong piezoelectric fields in [111]B InGaAs/GaAs strained quantum wells have been shown to have promising applications in optoelectronic devices. Blue shifts with applied voltages, lower operating voltages and large optical nonlinearities have been claimed [1-4]. The fact that the piezoelectric field in the wells opposes the barrier electric field adds new flexibility in devices designed using such heterostructures. Thus, when considering a PIN diode where multiple quantum wells (MQW's) are embedded into the I-region, the electric field profile in this region depends on parameters such as the number of quantum wells and the barrier thicknesses [5]. In fact, by a proper device design, the average electric field in the MQW region may have either the same (positive) or the opposite sense (negative) that the barrier field. The resultant electric field profile affects markedly the lifetime and screening effects of the photogenerated carriers.

A series of PIN devices with positive and negative average electric field in the MQW region were designed and fabricated by molecular beam epitaxy on [111]B substrates. In mole fraction ranged from 7% to 27%. Reference samples grown on a [100] oriented substrate were also fabricated. Photoluminescence and photocurrent spectrocopies allowed to determine the dependence of the piezoelectric field on the In mole fraction, and to validate the conduction band design rules. It was shown that, in the negative electric field devices, the carriers accumulate at the QW's at both ends of the active region, instead of being swiftly collected by the P^+/N^+ regions.

The time-resolved measurement of the optical nonlinearity formation and of the carrier dynamics was made by a pump and probe technique. A line shape analysis of the measured differential transmission spectra allowed the dynamics of the exciton to be clearly resolved. In a sample containing ten strained 10 nm wide $In_{0.15}Ga_{0.85}As$ quantum wells separated by barriers 15nm wide, designed to have a negative average electric field, the charge accumulated at the local potential minima causes a blue shift that sustains longer than 40μs after photoexcitation.

This study reveals that, in piezoelectric [111] MQW structures, the photocarriers dynamics and their screening effects depend critically on the conduction band profile, and specifically on the average electric field in the active MQW region.

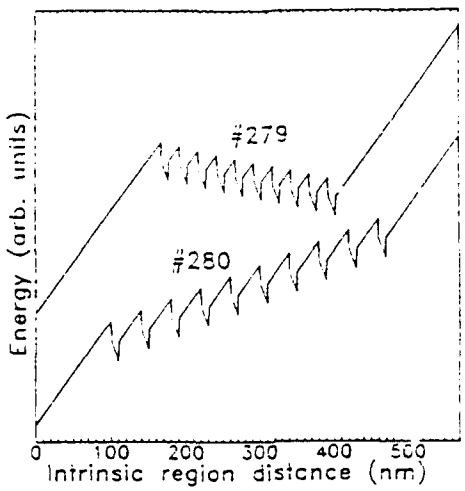

Figure 1.-PIN structures with positive and negative average electric field in the MQW region.

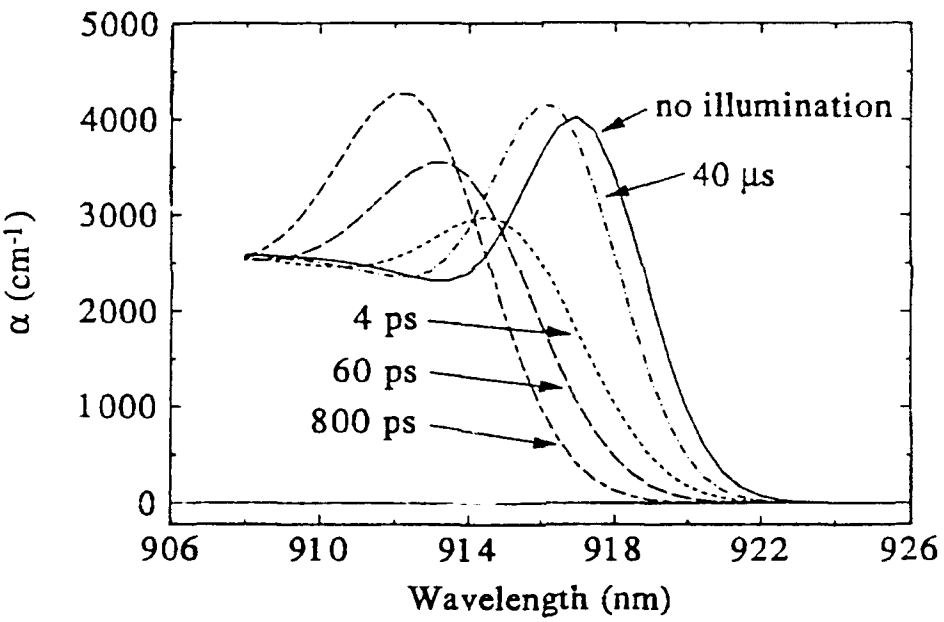

Figure 2.-Line shape analysis of the optical nonlinearities arisen in sample #279 performed with 3.2 ps (FWHM) pulses at intervals of 40 μs.

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GaInSb INFRARED PHOTODIODES GROWN BY MOLECULAR BEAM EPITAXY

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Abstract

We present a $Ga_{0.65}In_{0.35}Sb$ photodiode prepared by molecular beam epitaxy on GaAs (100) substrate. Grown PIN structures were processed into actual photodiode devices, using multiple litographic steps to define a $5x10^{-4}$ cm^2 diode area, with lateral insulation by mesa etching and SiO_2 PECVD passivation.

I-V characteristic corresponds to a good quality diode (ideality factor: 1.86) with current associated mainly to recombination in the intrinsic region. The leakage current at 300 K is 10^{-3} Amp/cm^2 for 0.1 V reverse bias and 10^{-1} Amp/cm^2 for 0.5 V reverse bias, one order of magnitude lower than in previous reported devices grown on GaSb substrates.

Measurements of wavelength response under photovoltaic mode (no external bias) have been carried out, using a monocromator, a chopped IR source and a GaSb fiter, in combination with lock-in detection. The GaInSb diode shows a cut-off wavelength of 2.5 μm in agreement with expected band gap at 300 K.

DESIGN OF A MULTIQUANTUM BARRIER USING AN EXTENDED EFFECTIVE MASS MODEL TO INCLUDE THE EFFECTS OF $\Gamma - X$ MIXING

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ABSTRACT

The performance of laser diodes operating in the visible region of the electromagnetic spectrum is limited by poor thermal characteristics. This is due mainly to carrier leakage over the relatively small barrier provided by the intrinsic conduction band offset. It has been proposed [1, 2] that the introduction of a multi-layer structure, known as a MultiQuantum Barrier (MQB), on the p-side of the laser active region could, by virtue of a quantum interference effect, provide an enhanced virtual barrier to carrier overflow. The advantage of such a system is to improve the confinement of carriers, thus leading to improved device performance [3, 4]. This also allows for the possibility of producing shorter wavelength lasers.

A problem with the high aluminium containing $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ alloys used in MQB structures is the proximity, in energy, of the Γ and X minima. To accurately describe the transmission of electrons through MQBs it is necessary therefore to take account of the $\Gamma - X$ mixing induced by the presence of interfaces. A phenomenological approach is used to extend the well known effective mass approximation to include a mixing of states, the strength of which is determined solely by a mixing parameter Δ. The Schrödinger equation for such a system is given in Equation 1.

$$\begin{pmatrix} \frac{\hbar^2 \cdot k^2}{2m_X^*} + E_X & \Delta \\ \Delta & \frac{\hbar^2 \cdot k^2}{2m_\Gamma^*} + E_\Gamma \end{pmatrix} \begin{pmatrix} \Psi_X \\ \Psi_\Gamma \end{pmatrix} = E \cdot \begin{pmatrix} \Psi_X \\ \Psi_\Gamma \end{pmatrix} \tag{1}$$

where m_X^* and m_Γ^* are the effective masses of the electron in the X and Γ conduction band states and E_X, E_Γ are the X and Γ conduction band minima respectively.

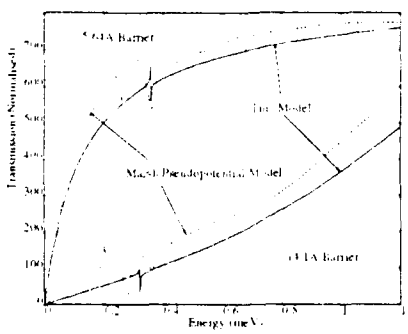

Figure 1: *Comparison of the extended effective mass model with empirical pseudopotential model of Marsh [5] for GaAs/AlAs single barrier of thickness* $5.64\AA$ *and* $14.1\AA$.

In figure 1 a comparison is made between the extended effective mass model and an empirical pseudopotential model developed by Marsh [5]. Excellent agreement is shown, given the simplicity of the extended effective mass model. This model is then used to show the improvement in carrier confinement a MQB can provide over a single barrier of same total thickness. For an appropriate design a doubling of effective barrier height can be achieved. See Figs. 2 and 3. However, it can be shown that for a given MQB there exists a threshold in the conduction band offset, below which the MQB cannot provide any barrier enhancement. The model is thus shown to provide a useful design tool in the development of MQBs.

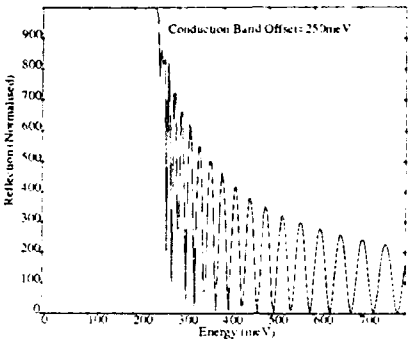

Figure 2: *Electron reflection from a single barrier of same total thickness as the optimised MQB design.*

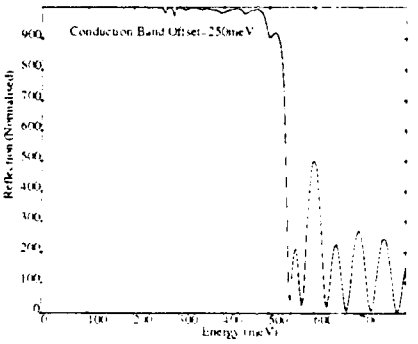

Figure 3: *Enhanced electron reflection from designed multiquantum barrier.*

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